

Compal Confidential

Z5WAE Schematics Document

AMD "Beema" Platform

AMD 25W APU With Puma+ Core and 25W-DGPU with Jet

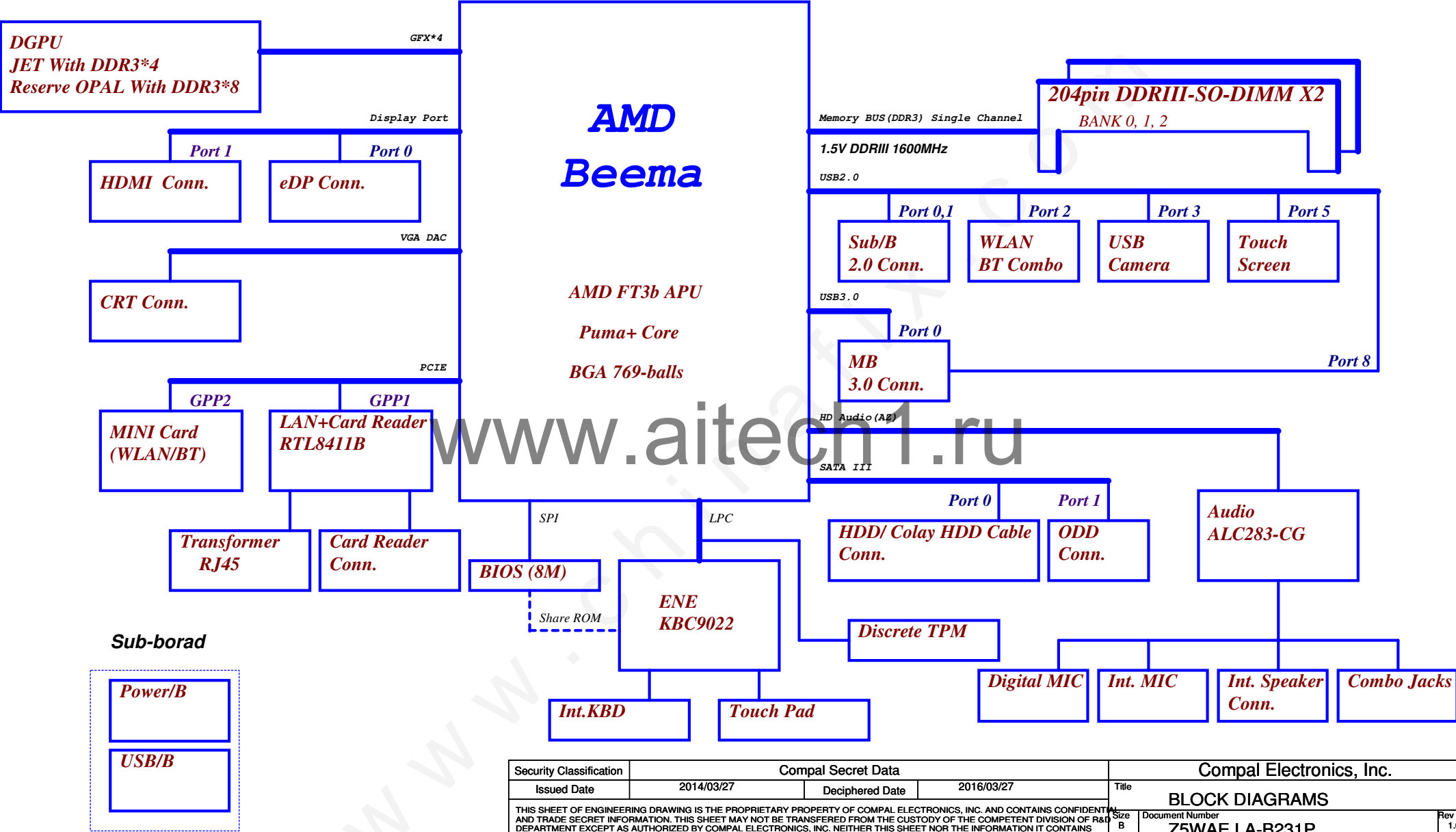
LA-B231P REV: 1.0

2014-03-27

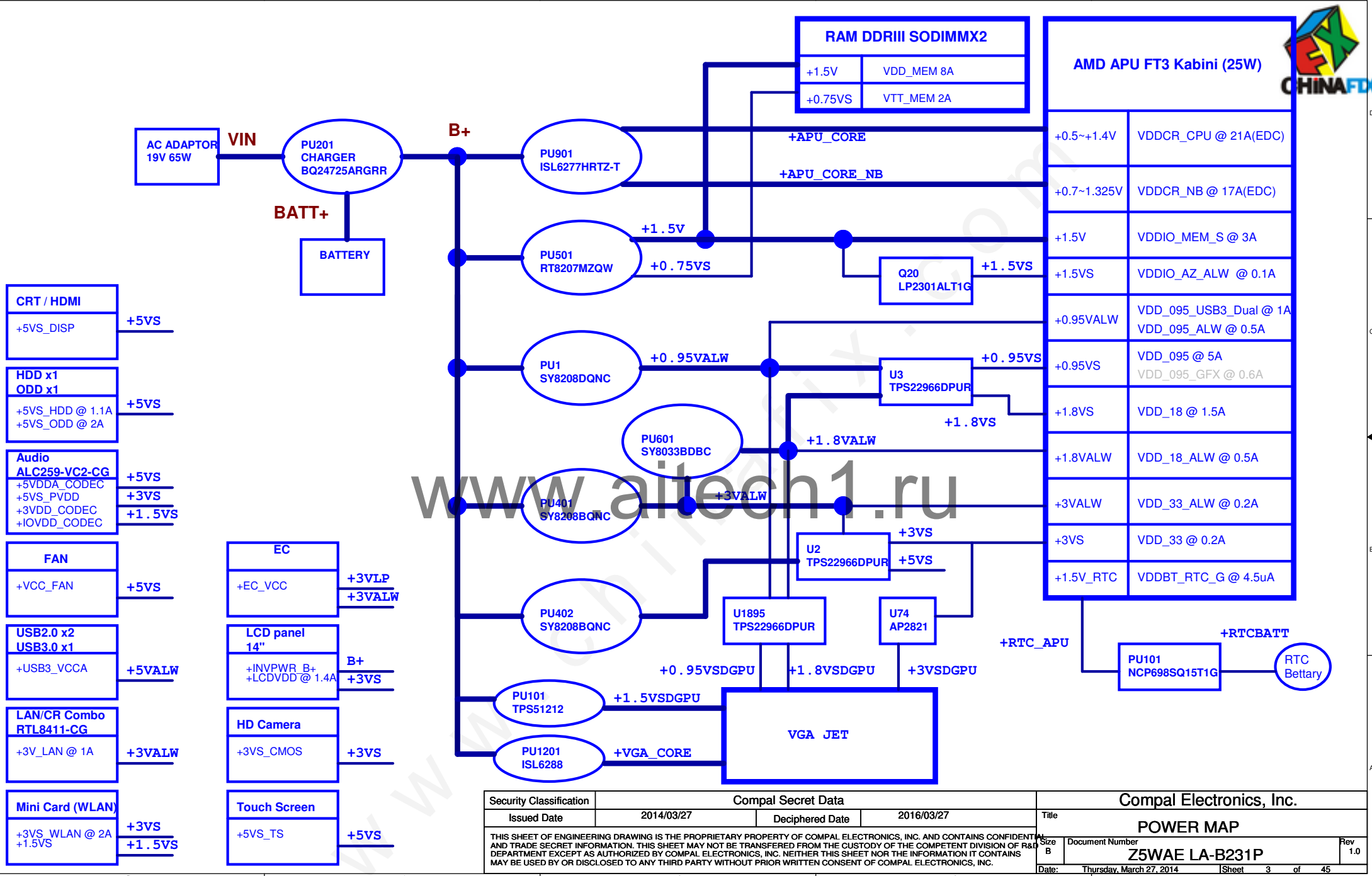
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Model Name : Z5WAE



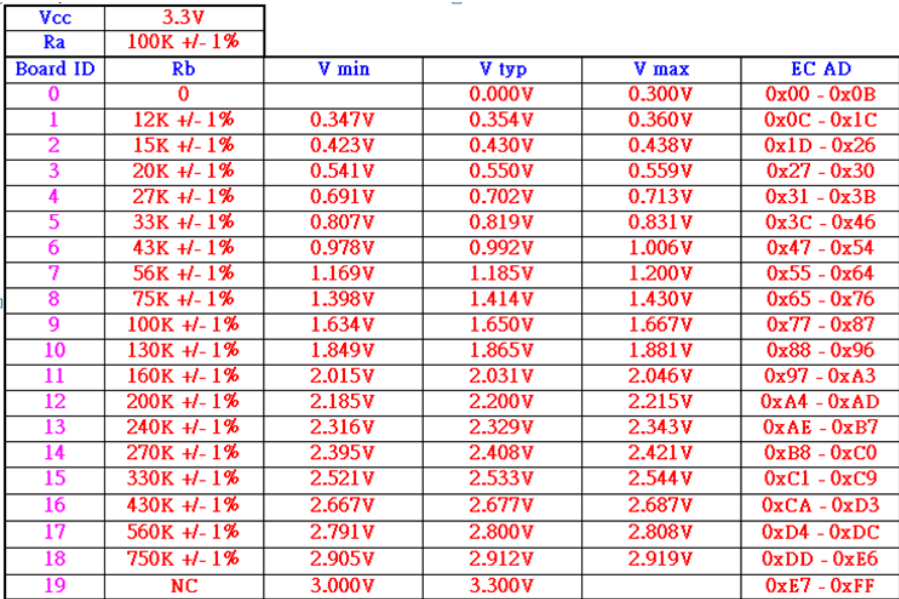
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Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	OFF	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+0.95VSDGPU	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H
			VGA Temp.		41H



BOM Structure	BTO Item
@	Unpop
CONN@	Connector part control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
AL@	Auto Load EC ROM
RS@	R-short
JP@	Jump
TP@	Test point
SP@	Short pad for clear CMOS
1DMIC@	Use 1 DMIC
2DMIC@	Use 2 DMIC
45@	HDMI royalty
9012@	Use KBC9012
9022@	Use KBC9022
A6@	Use A6 APU
E1@	Use E1 APU
BL@	Keyboard backlight
TPM@	Use discrete TPM module
TPUSB@	Use USB to I2C IC for T/P
TPSM@	Use APU SMBus for T/P
VGA@	Have discrete graphic
MARS@	Use Opal
JET@	Use Jet
128@	Dual channel VRAM,pop with MARS@
X76@	VRAM type select,control by X76XX@
X76XX@	VRAM type select, control level X76

Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	
4	
5	
6	
7	



<i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1 (Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

G-A ———— +RTC
EC_ON

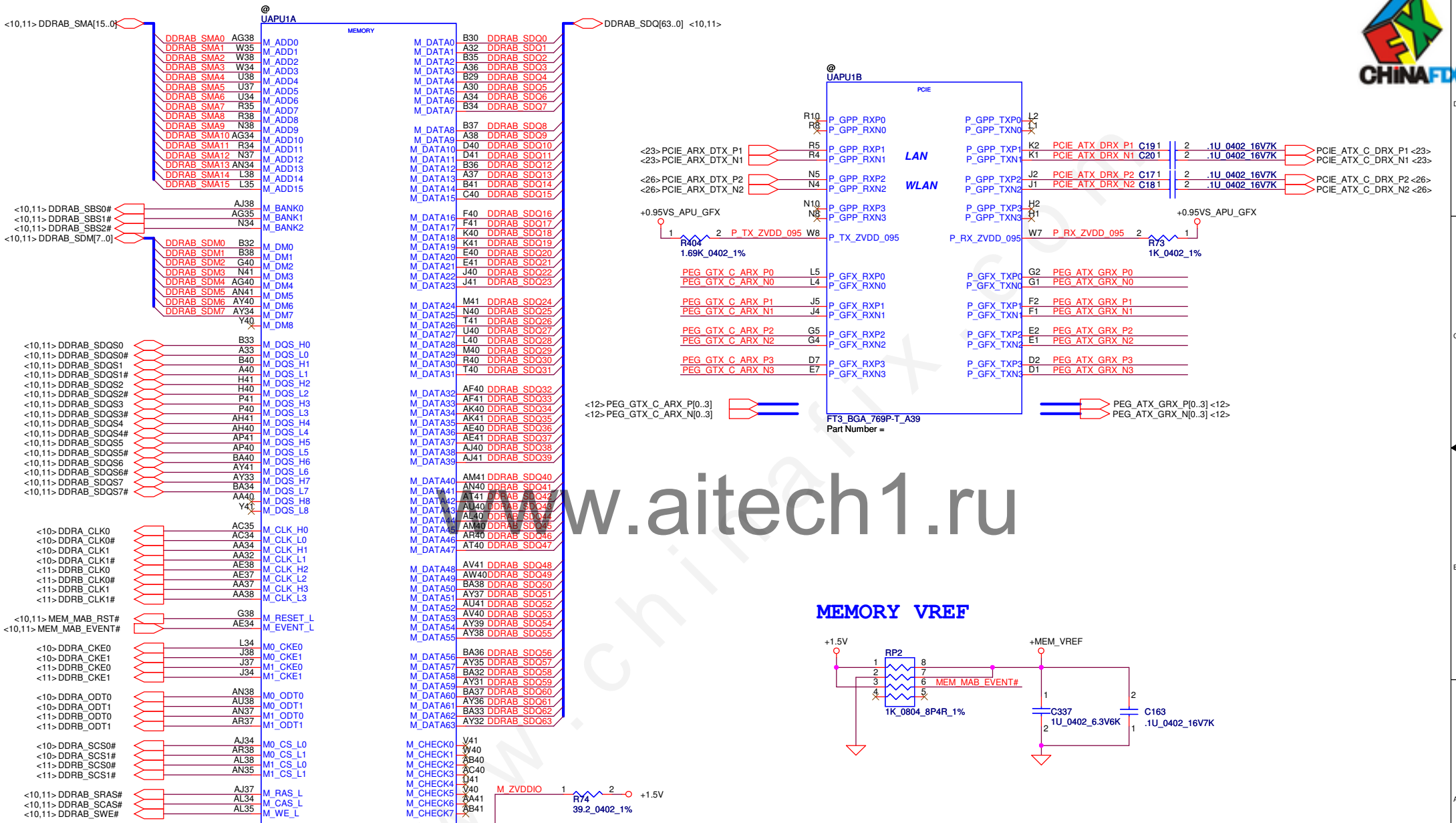
G-B ———— +3VALW/+5VALW
+1.8VALW
+0.95VALW
SYSON

G-C ———— +1.5V
SUSP#

G-D ———— +3VS
+1.8VS
+1.5VS
+0.95VS
VR_ON

G-E ———— +APU_CORE
+APU_CORE_NB

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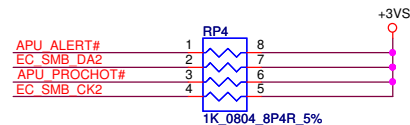
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HDMI

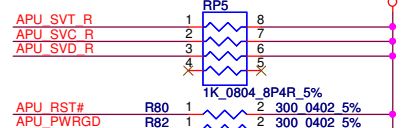
eDP

CRT

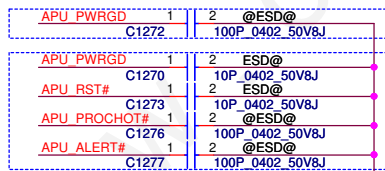
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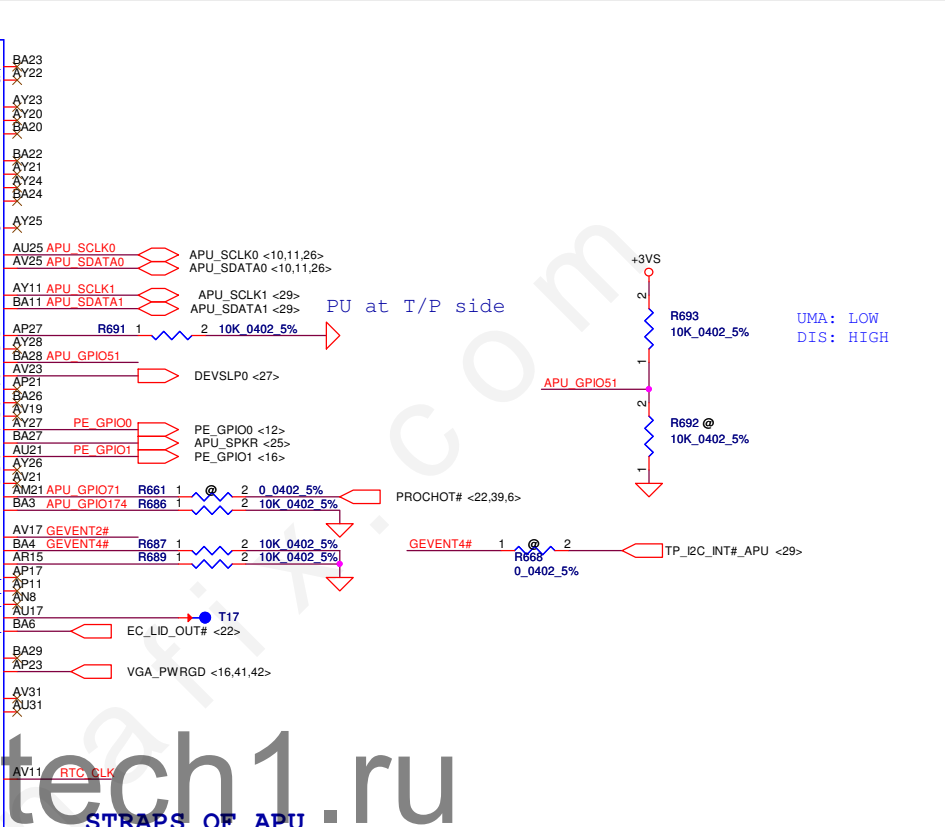
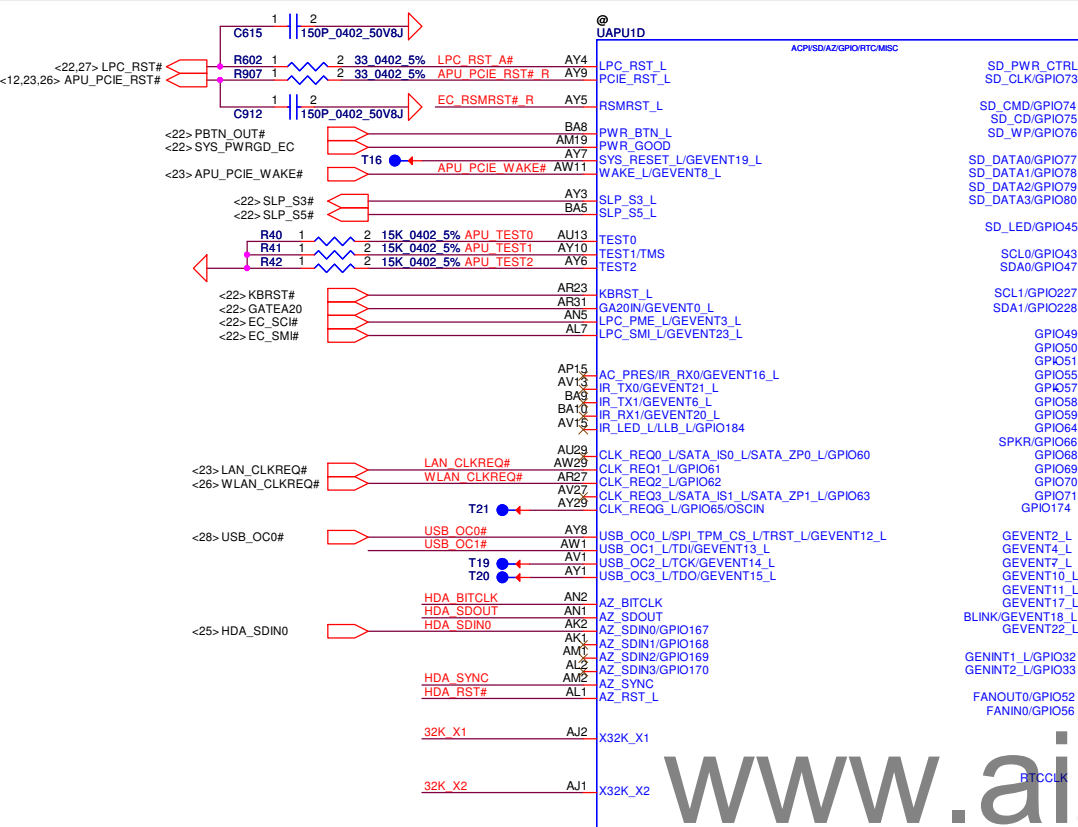
PU +1.8VS



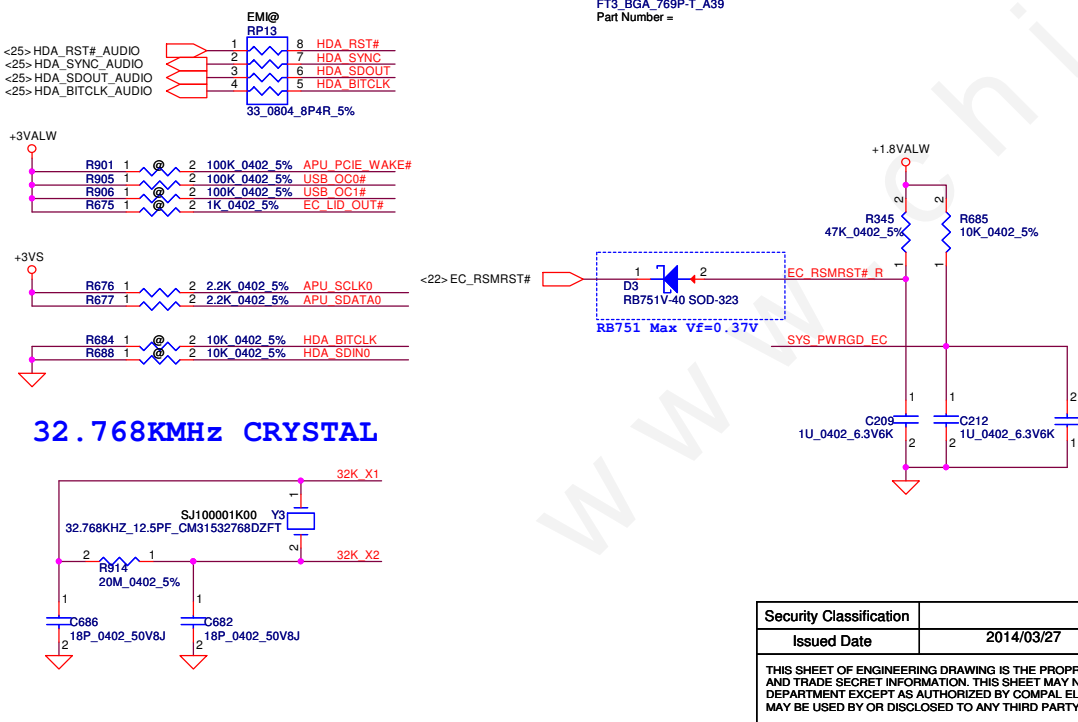
Close To PU801
Close To APU's Pin



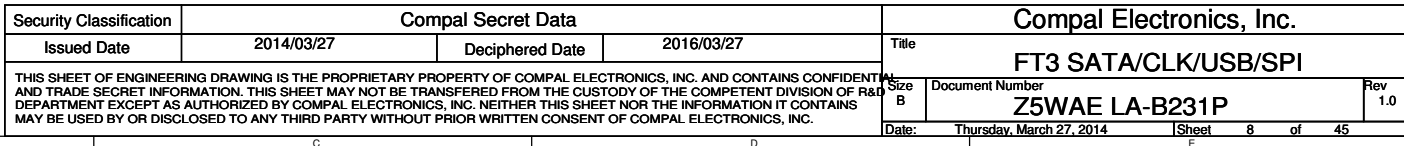
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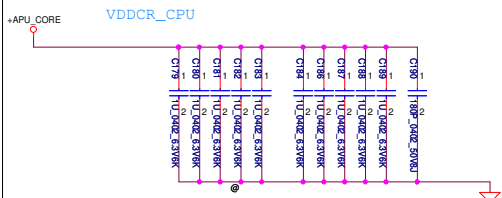
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMIN (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMIN FOR SIMULATION



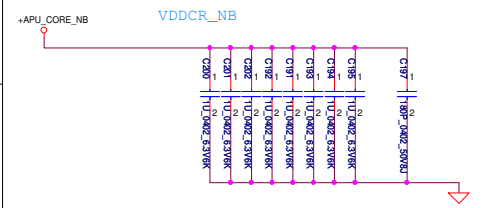
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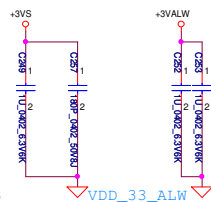
CORE POWER OF APU



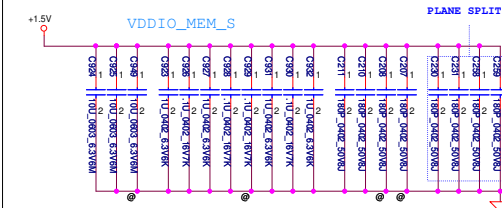
INTEGRATED GPU POWER OF APU



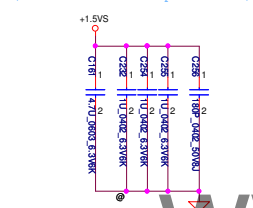
+3VALW/+3VS OF APU



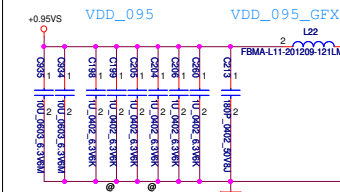
+1.5V/+1.5VS OF APU



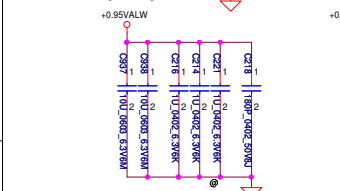
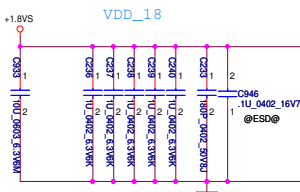
VDDIO_AZ_ALW
(Could be S0 or S5 power rail)



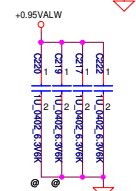
+0.95VALW/+0.95VS OF APU



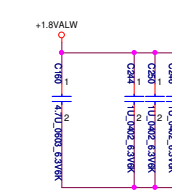
+1.8VALW/+1.8VS OF APU



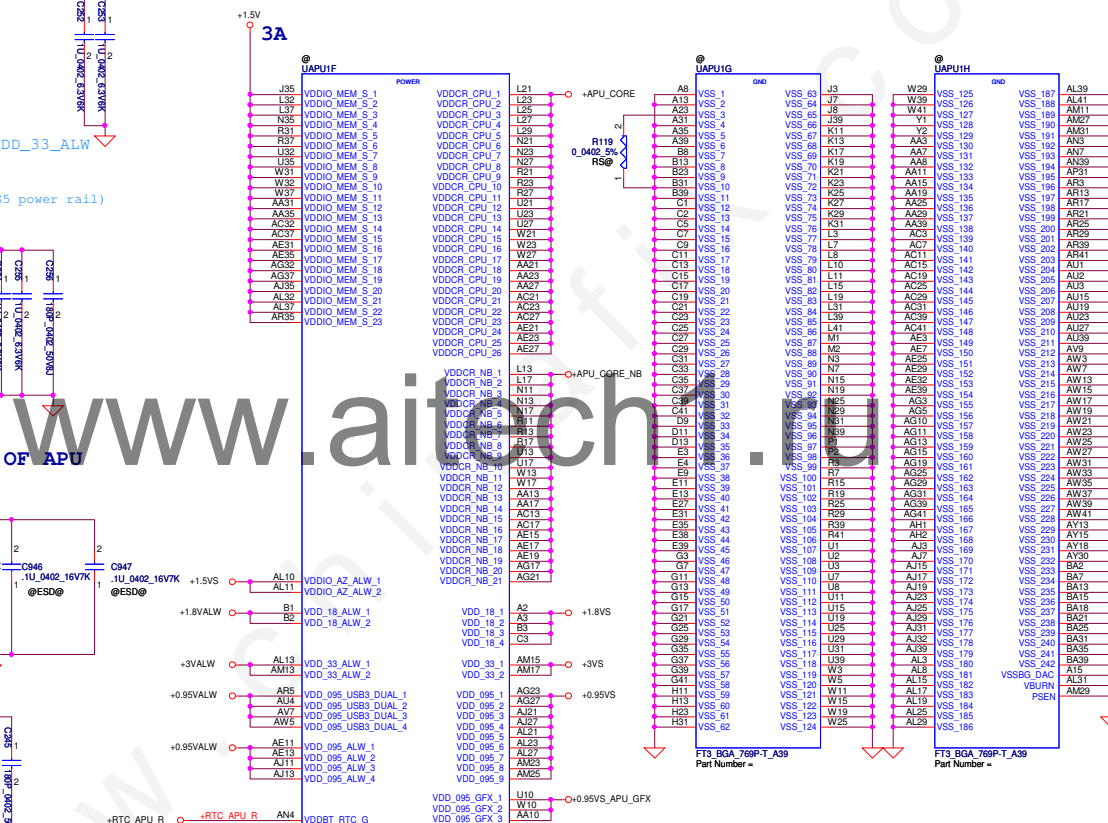
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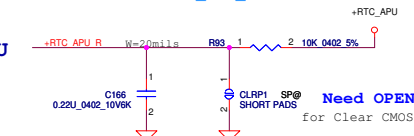
VDD 095 ALW



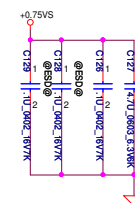
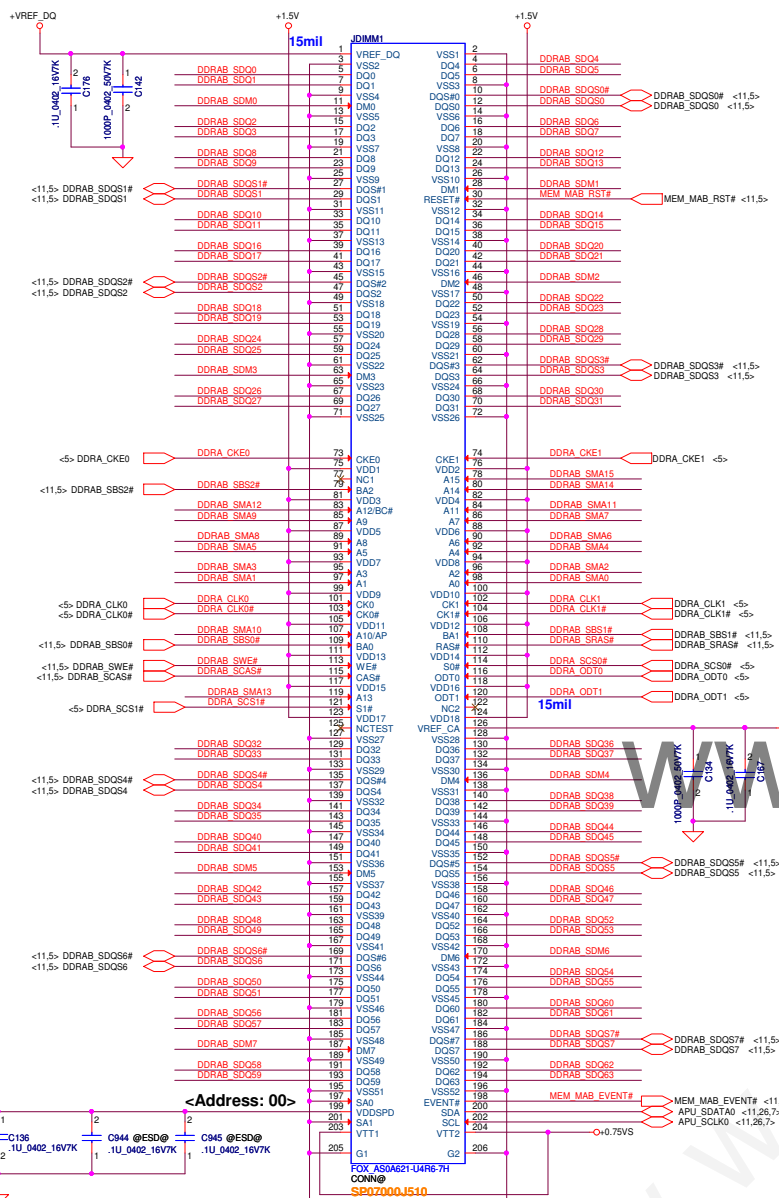
VDD 18 ALW



RTC OF APU

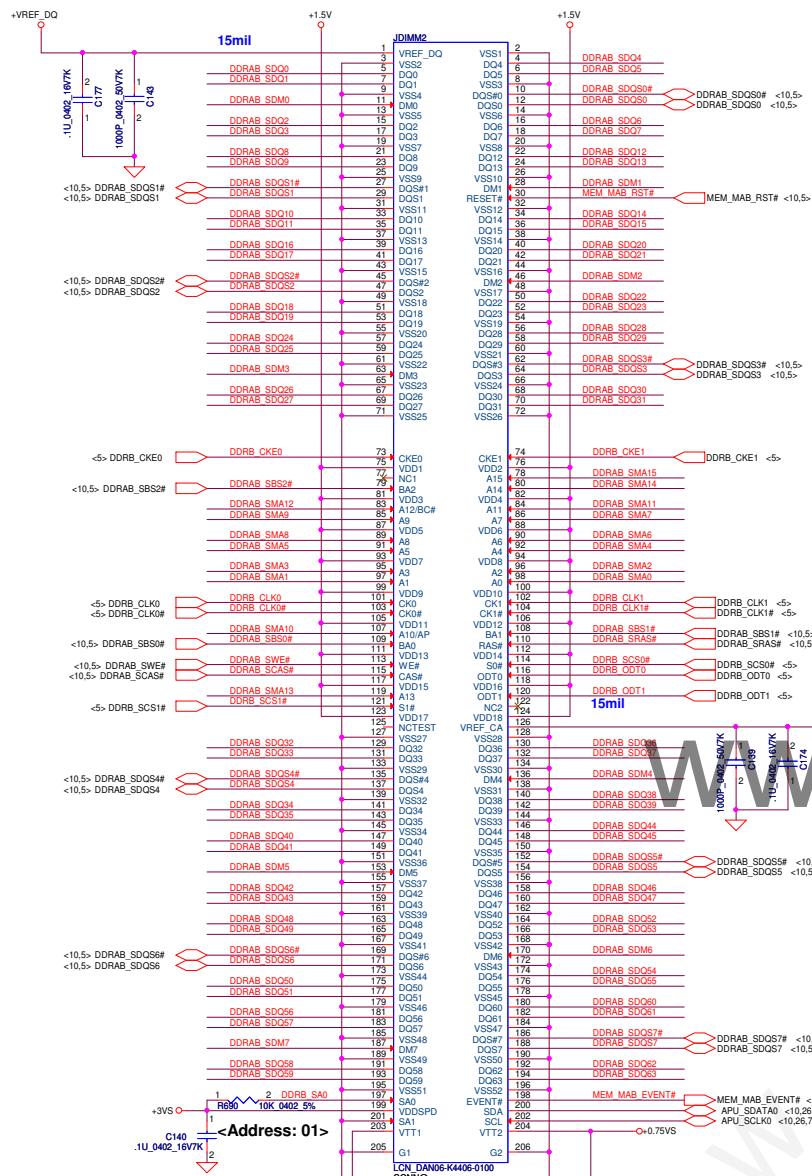


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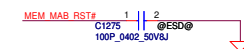
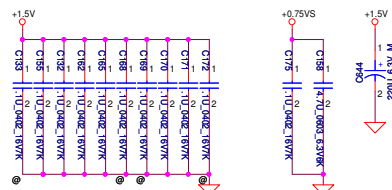
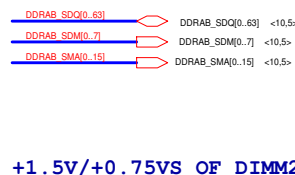


DIMM A H:4mm RVS

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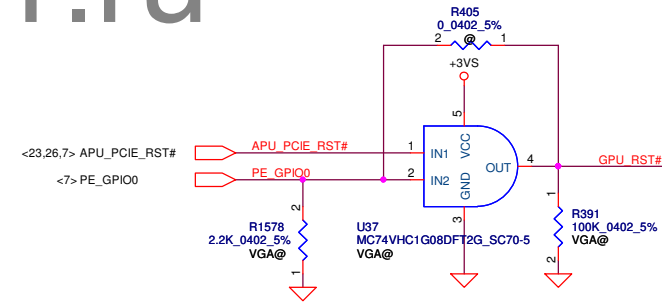
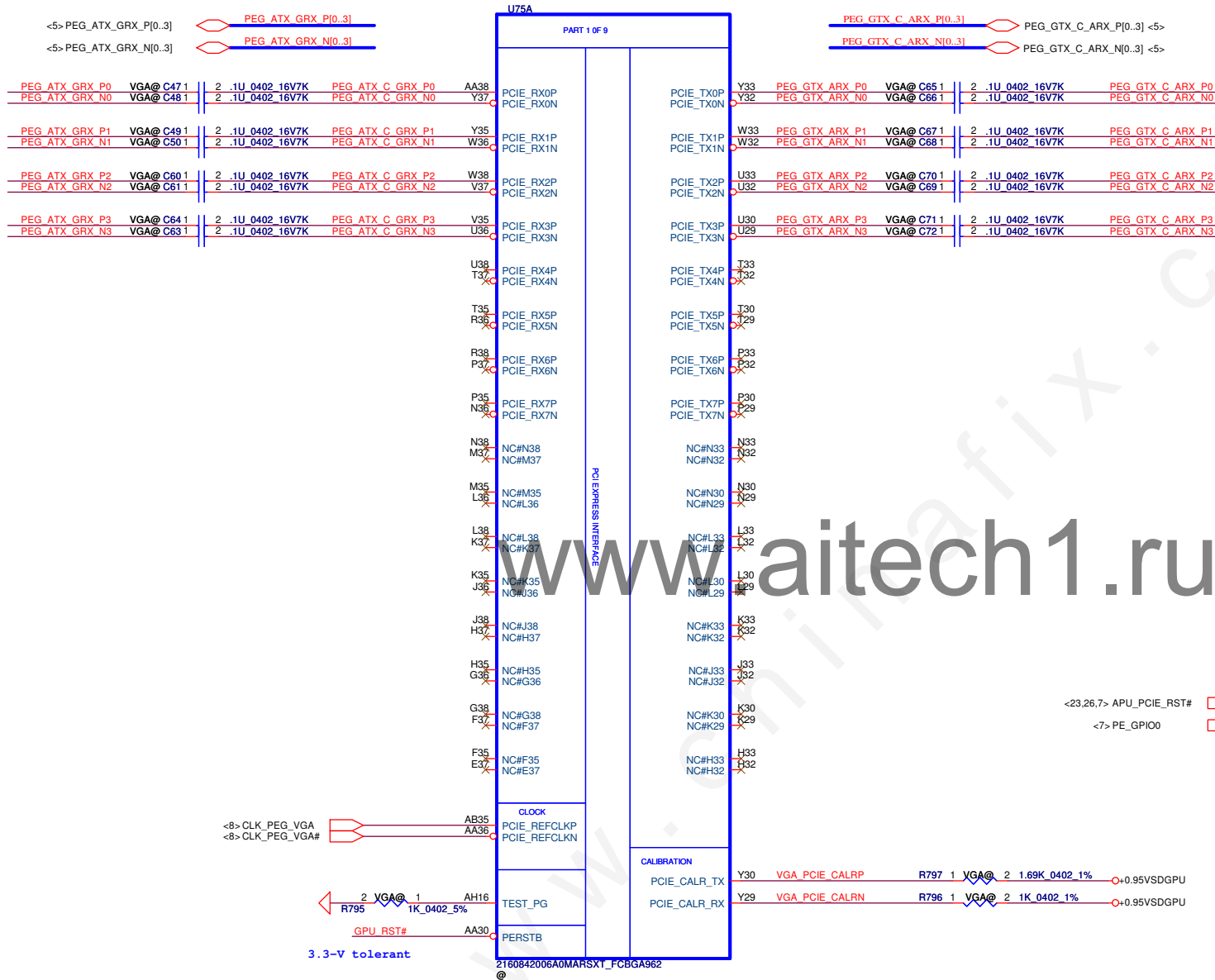


DIMM_B H:4mm STD



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GFX PCIE LANE REVERSAL



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SM010030010 200ma
120ohm/100mhz DCR 0.2

Mars MLPS configuration				
Bits[5:1]	PU(1%)	PD(1%)	Cap	
xx000	NC	4.75k		
xx001	8.45k	2.00k		
xx010	4.53k	2.00k		
xx011	6.98k	4.99k		
xx100	4.53k	4.99k		
xx101	3.24k	5.62k		
xx110	3.40k	10.0k		
xx111	4.75k	NC		
00xxx			680nF	
01xxx			82nF	
10xxx			10nF	
11xxx			NC	

PS0[1]=1 : same as GPIO_11 Since the frame buffer size is 512 MB
PS0[2]=0 : same as GPIO_12 the aperture size is set to 256 MB.
PS0[3]=0 : same as GPIO_13
PS0[4]=1 : Reserved for internal use only. Must be 1
PS0[5]=1 : AUD_PORT_CONN_PINSTRAP[0]

100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2Mbit M25P20 (ST)
101 - 4Mbit M25P40 (ST)
101 - 8Mbit M25P80 (Chingis)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)

PS_1[1] = 0 : PCIeR GEN3 is not supported.
PS_1[2] = 0 : Reserved for internal use only
PS_1[3] = 0 : Reserved for internal use only
PS_1[4] = 1 : TX_PWRB_ENB: Full Tx output swing.
PS_1[5] = 1 : TX_DEMPH_EN: Tx deemphasis enabled.

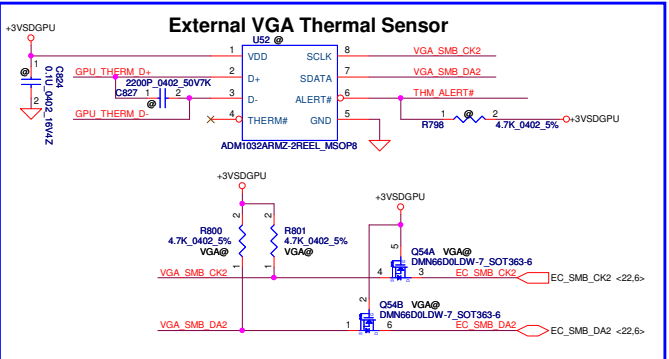
PS_2[1] = 0 : Reserved.
PS_2[2] = 0 : Reserved.
PS_2[3] = 0 : BIOS_ROM_EN :Disable the external BIOS ROM device.
PS_2[4] = 0 : VGA_DIS = 0:VGA controller capacity enabled.
PS_2[5] = 1 : Reserved.

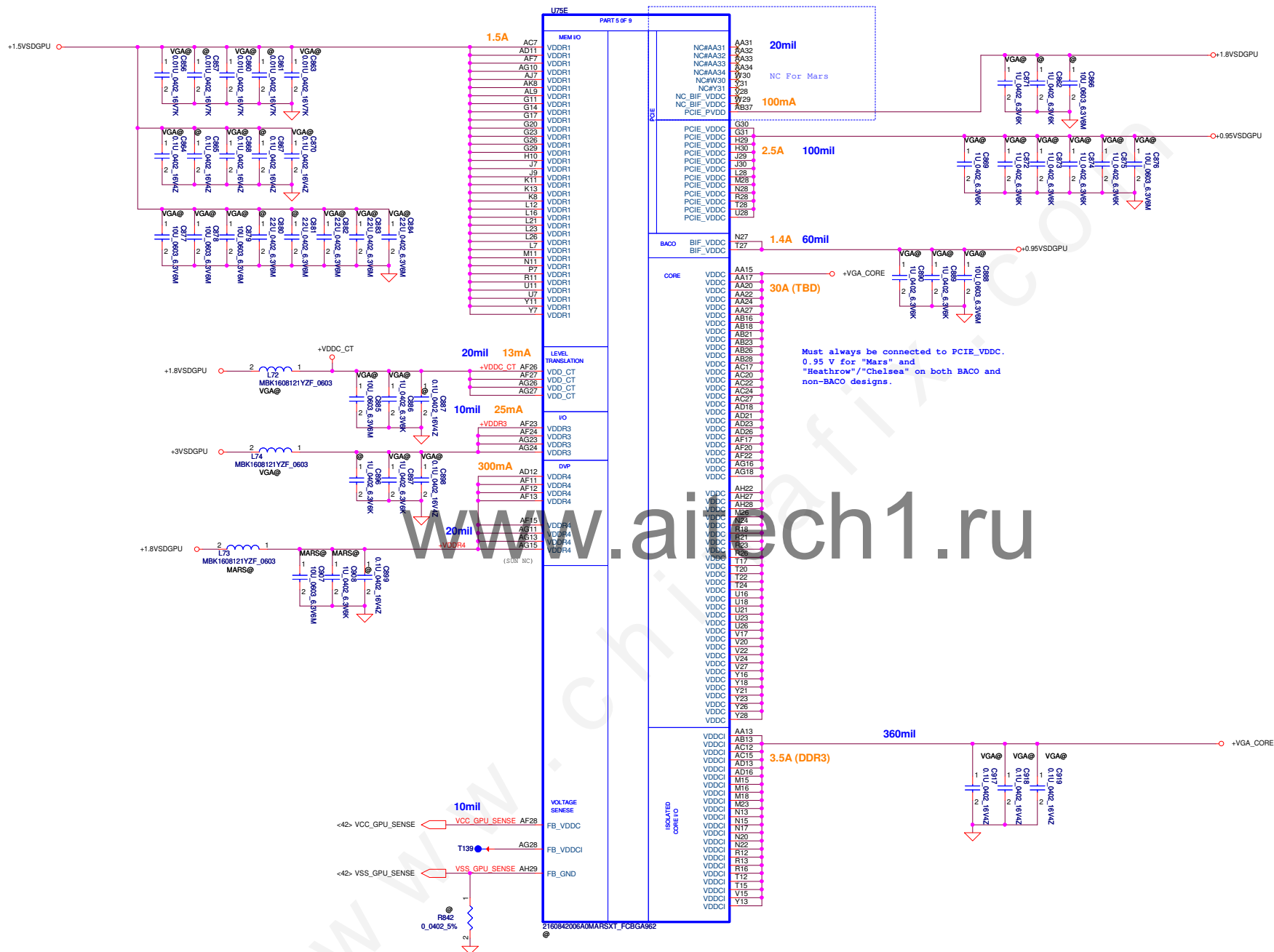
PS_3[1] = x :
PS_3[2] = x : VRAM ID
PS_3[3] = x :
PS_3[4] = 1 : AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] = 1 : AUD_PORT_CONN_PINSTRAP[2]

===== VRAM ID for Jet =====

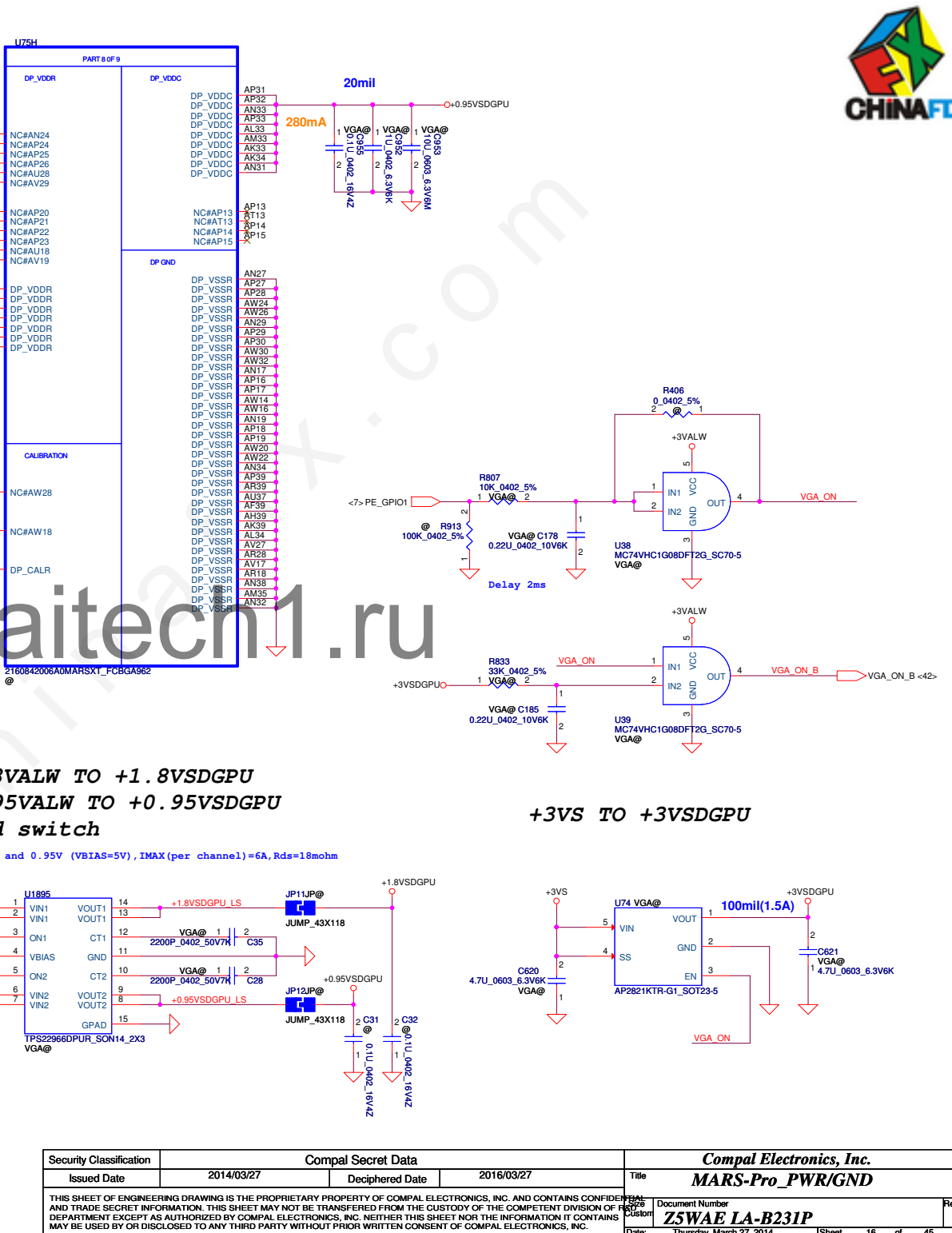
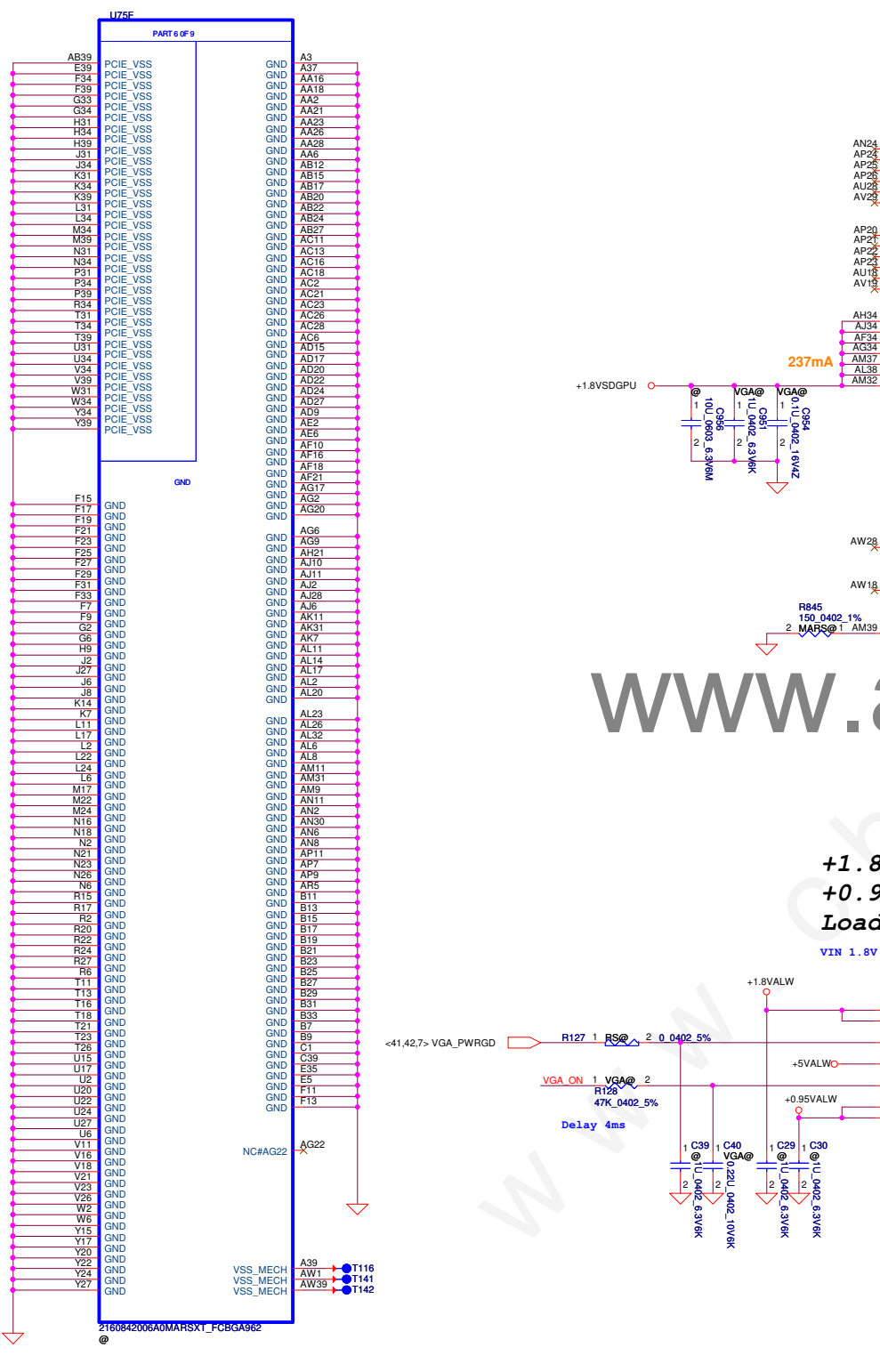
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001 Micron S IC D3 128M16 MT41J128M16JT-093G:K*4(SA000067550)
010 Samsung S IC D3 128M16 K4W2G16460-BC1A*4(SA000068090)
011 Hynix S IC D3 256M16 H5PC4G63APF-11C*4(SA000068840)
100 Micron S IC D3 256M16 MT41J256M16HA-093G:E*4(SA000077K20)
101 Samsung S IC D3 256M16 K4W4G16460-BC1A*4(SA000077P20)

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				Custom	Z5WAE LA-B231P	1.0
				Date:	Thursday, March 27, 2014	Sheet 13 of 45



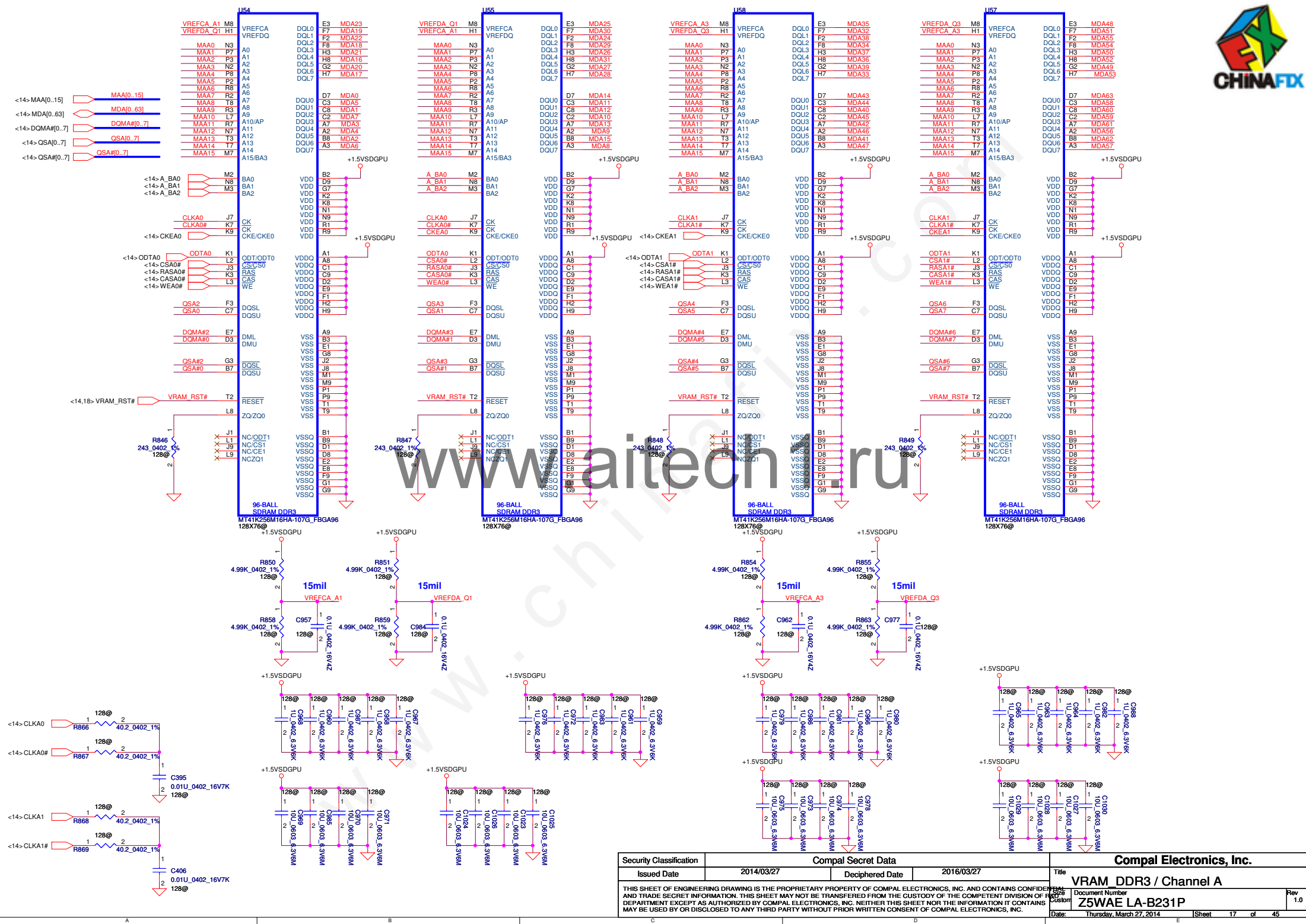


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The figure is a detailed PCB layout for a 96-BALL SDRAM DDR3, showing four channel configurations (U54, U55, U58, U57) with detailed pin connections, power planes, and component footprints. The layout includes a legend for signal types, a security classification table, and a title block with company information.

Legend:

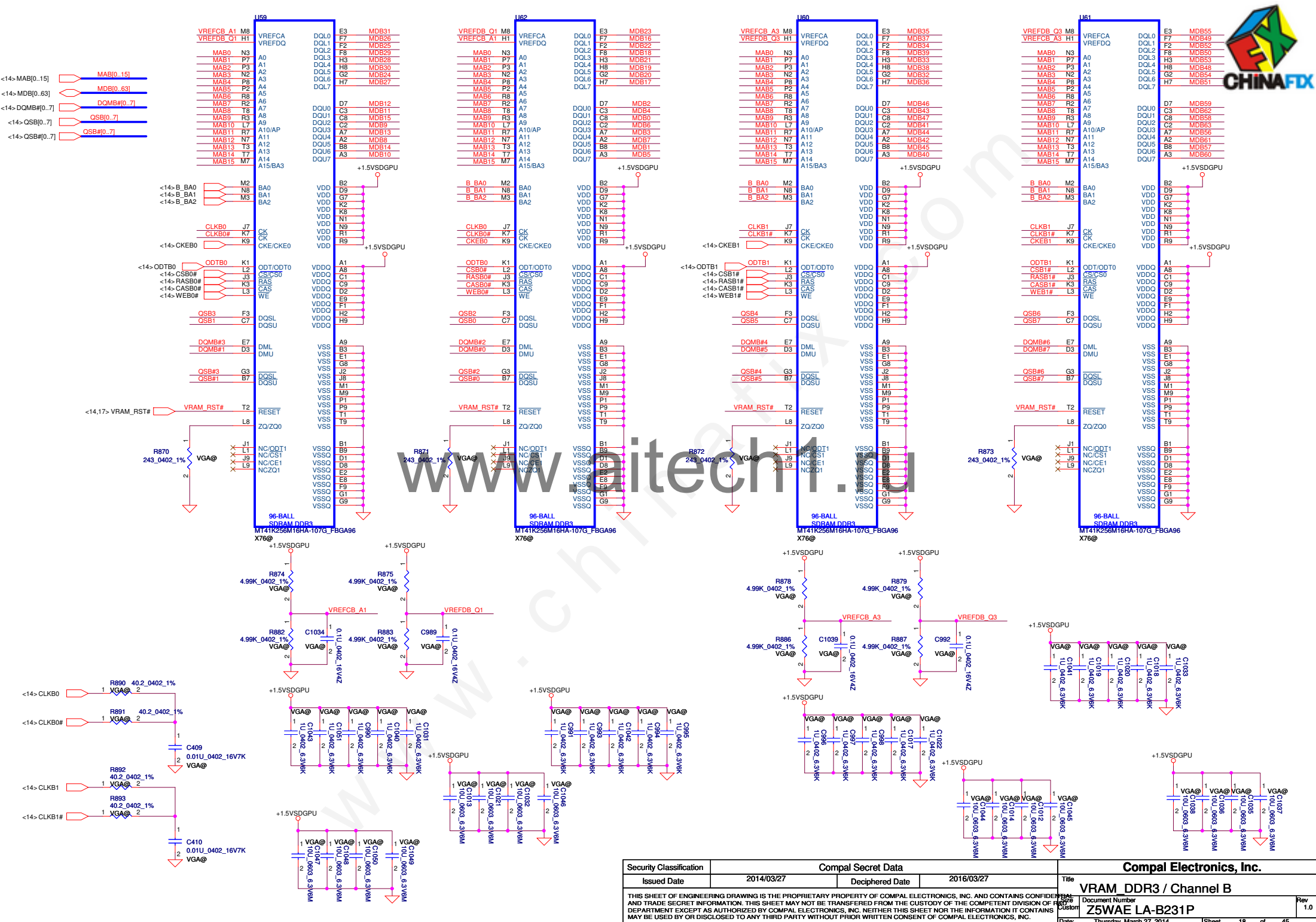
- <14> MAA[0..15] (Blue)
- <14> MDA[0..63] (Blue)
- <14> DQMA[0..7] (Blue)
- <14> QSA[0..7] (Blue)
- <14> QSA# [0..7] (Blue)
- <14> A_BA0 (Blue)
- <14> A_BA1 (Blue)
- <14> A_BA2 (Blue)
- <14> CKEA0 (Blue)
- <14> ODTA0 (Blue)
- <14> CSA0# (Blue)
- <14> RASA0# (Blue)
- <14> CASA0# (Blue)
- <14> WEA0# (Blue)
- <14> QSA2 (Blue)
- <14> QSA0 (Blue)
- <14> DOMA#2 (Blue)
- <14> DOMA#0 (Blue)
- <14> QSA#2 (Blue)
- <14> QSA#0 (Blue)
- <14,18> VRAM_RST# (Blue)
- <14> CLKA0 (Blue)
- <14> CLKA0# (Blue)
- <14> CLKA1 (Blue)
- <14> CLKA1# (Blue)

Security Classification Table:

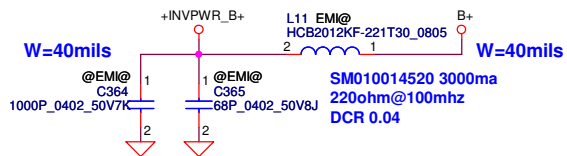
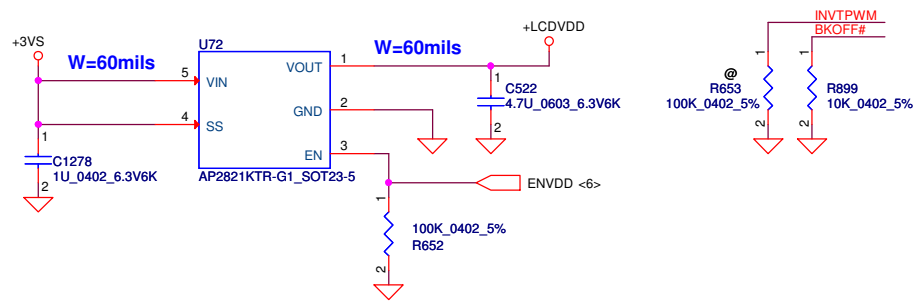
Security Classification	Compal Secret Data
Issued Date	2014/03/27
Deciphered Date	2016/03/27

Title Block:

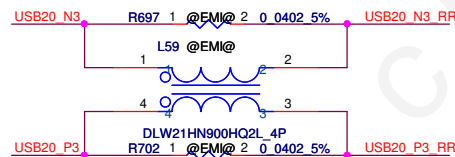
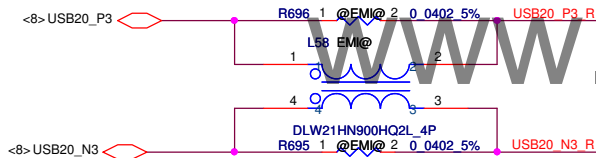
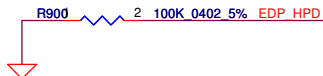
Compal Electronics, Inc.	
Title	Document Number
VRAM_DDR3 / Channel A	Z5WAE LA-B231P
Date	Thursday, March 27, 2014
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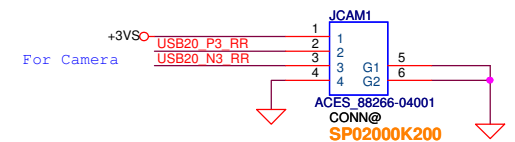
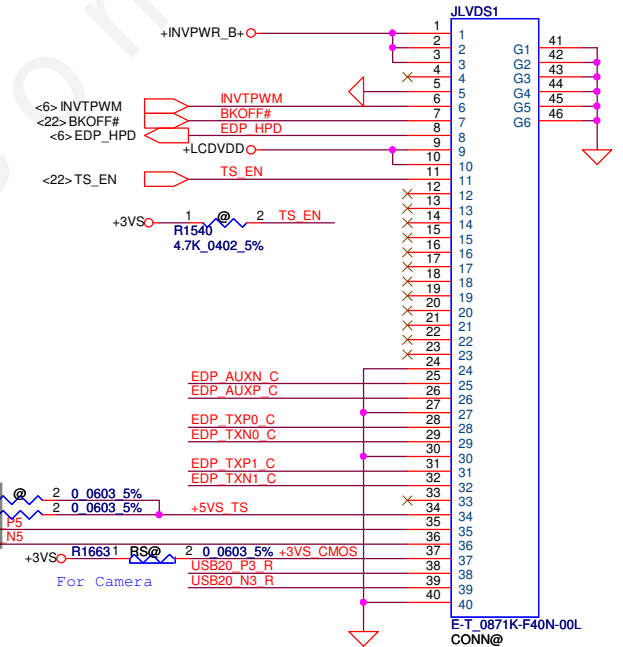
LCD POWER CIRCUIT



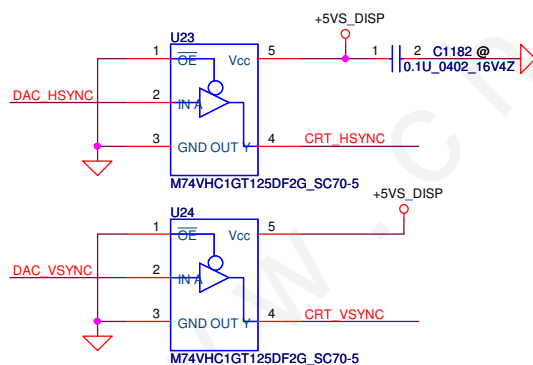
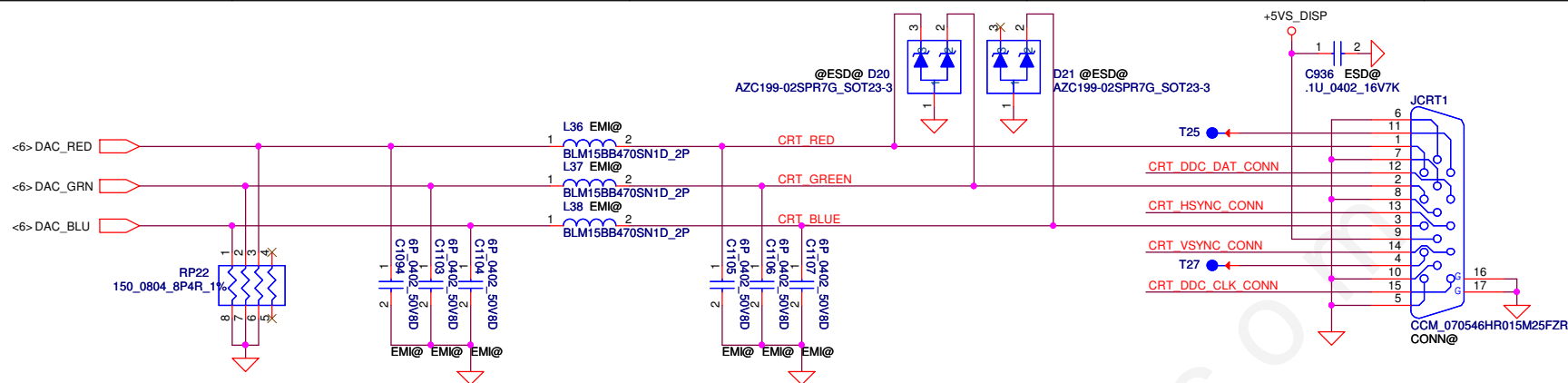
<6> EDP_TXP0	EDP_TXP0	C27 1	2	.1U 0402 16V7K	EDP_TXP0 C
<6> EDP_TXN0	EDP_TXN0	C33 1	2	.1U 0402 16V7K	EDP_TXN0 C
<6> EDP_TXP1	EDP_TXP1	C34 1	2	.1U 0402 16V7K	EDP_TXP1 C
<6> EDP_TXN1	EDP_TXN1	C36 1	2	.1U 0402 16V7K	EDP_TXN1 C
<6> EDP_AUXN	EDP_AUXN	C44 1	2	.1U 0402 16V7K	EDP_AUXN C
<6> EDP_AUXP	EDP_AUXP	C45 1	2	.1U 0402 16V7K	EDP_AUXP C



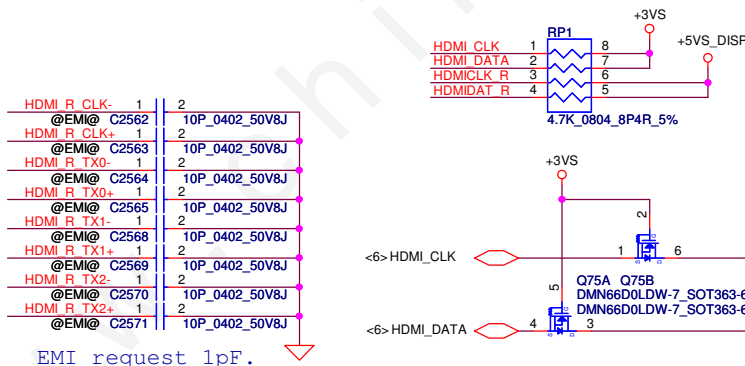
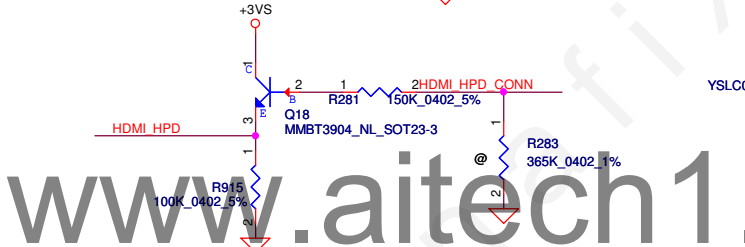
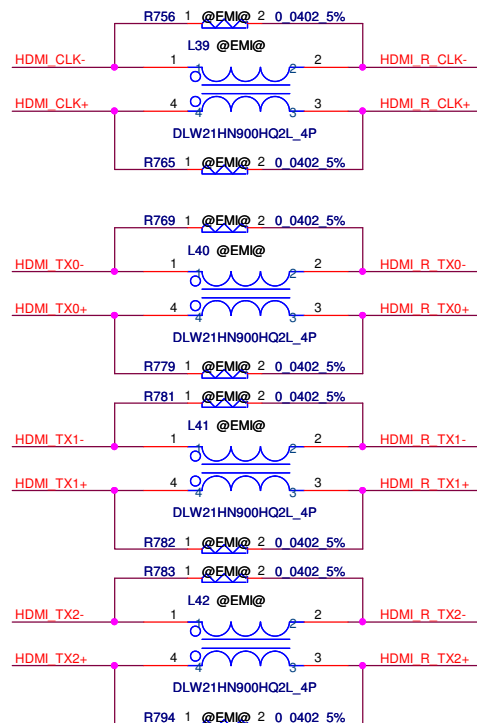
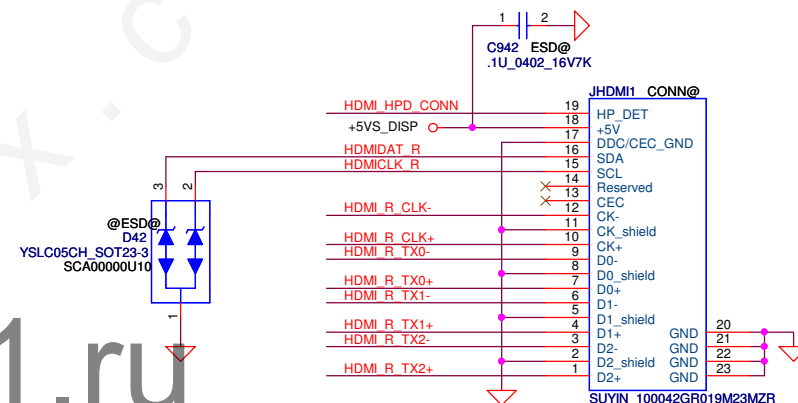
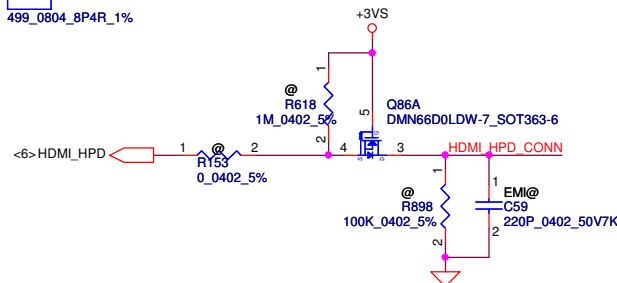
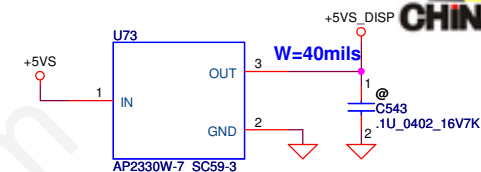
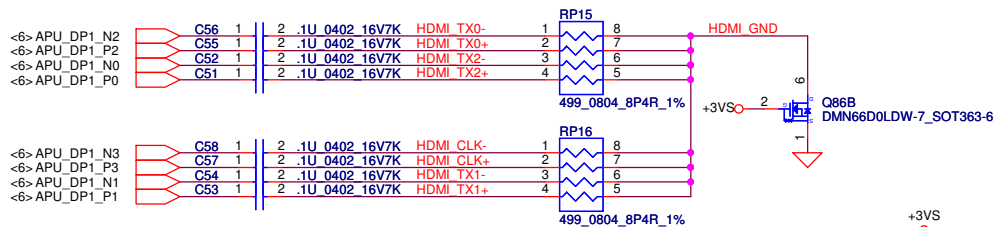
eDP PANEL Conn.



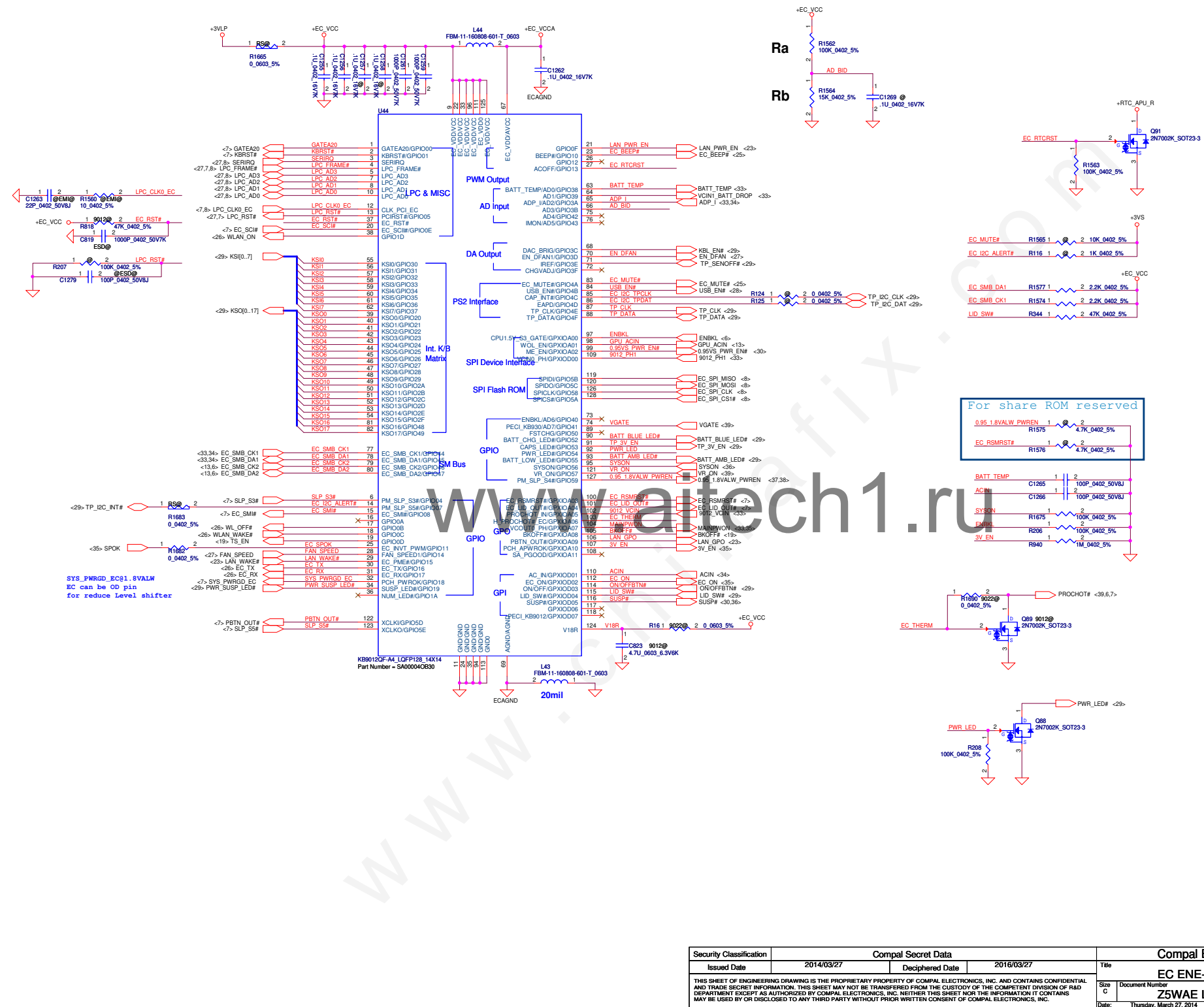
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	
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				Date: Thursday, March 27, 2014	Sheet 19 of 45

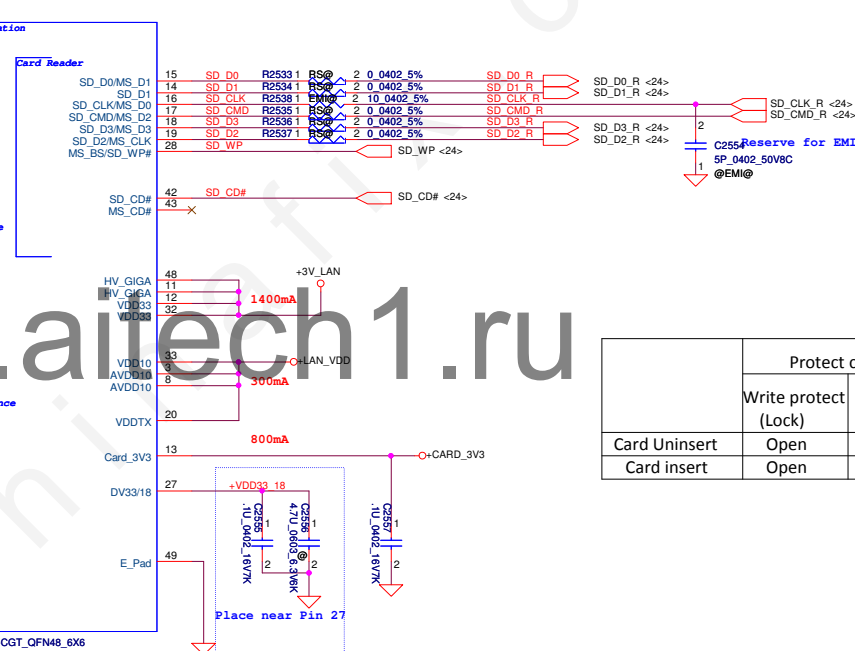
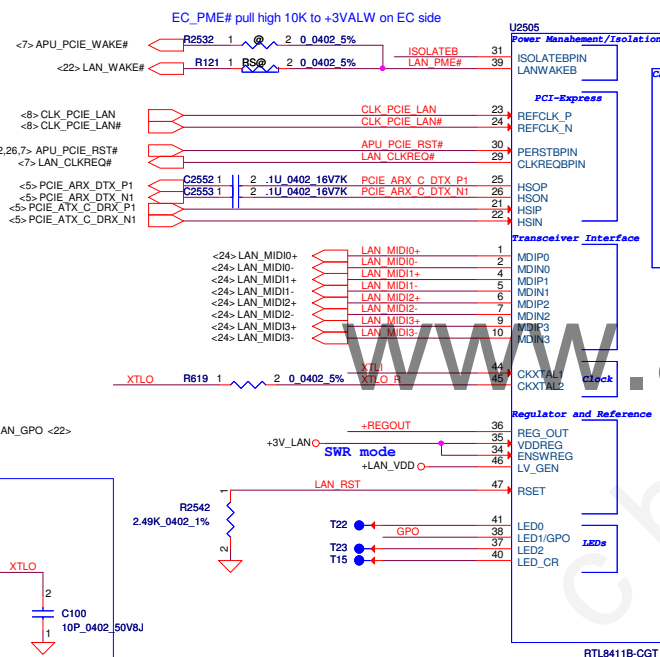
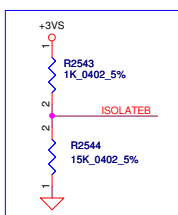
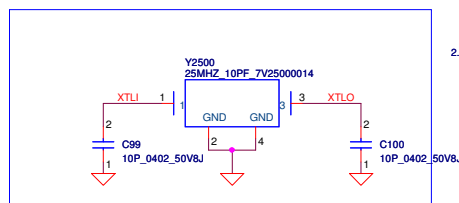
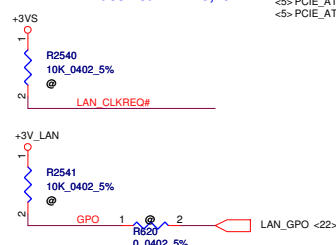
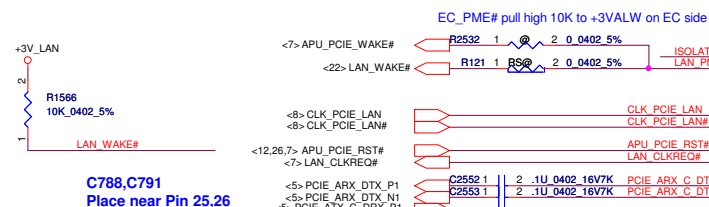
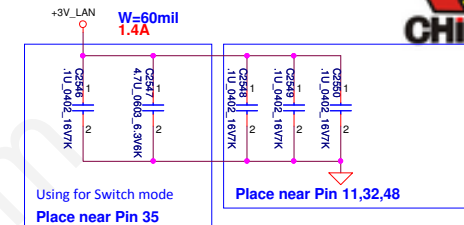
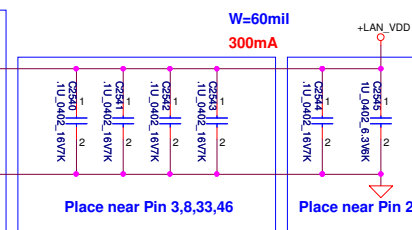
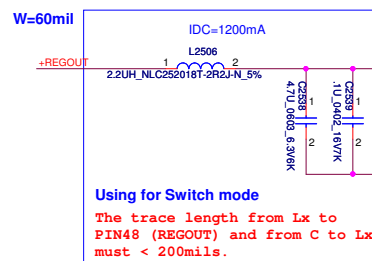
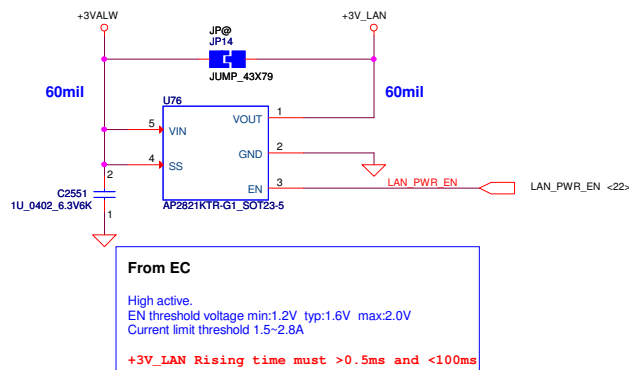


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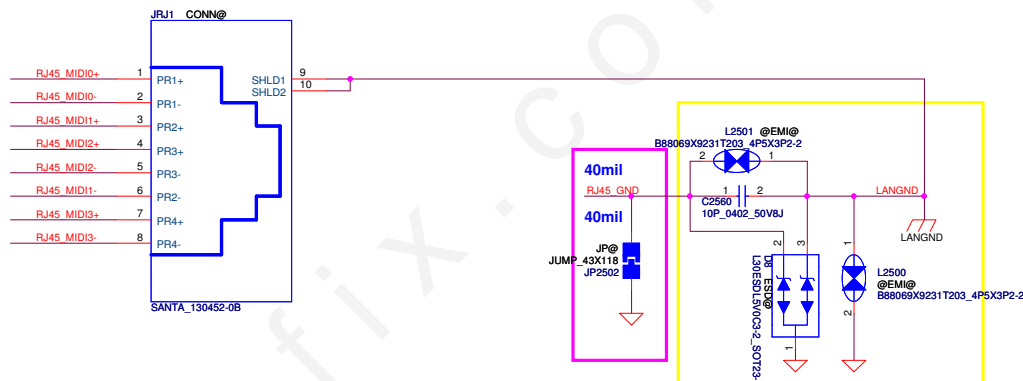
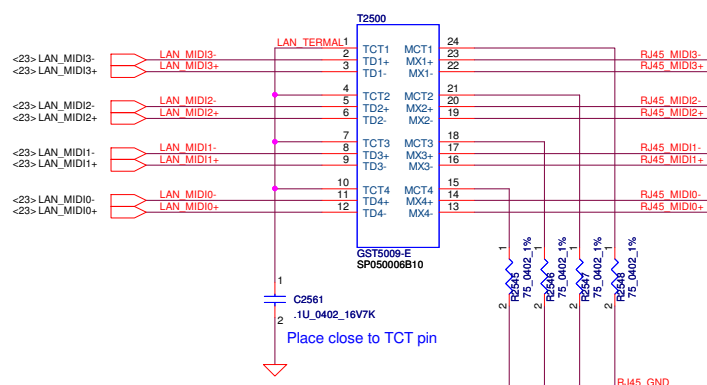
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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	
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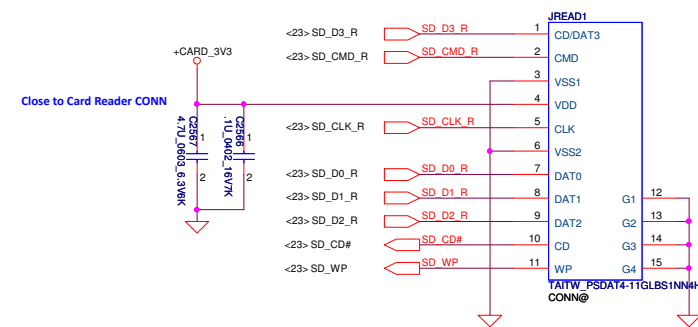
	Protect cotact		Card contac
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

LAN Connector



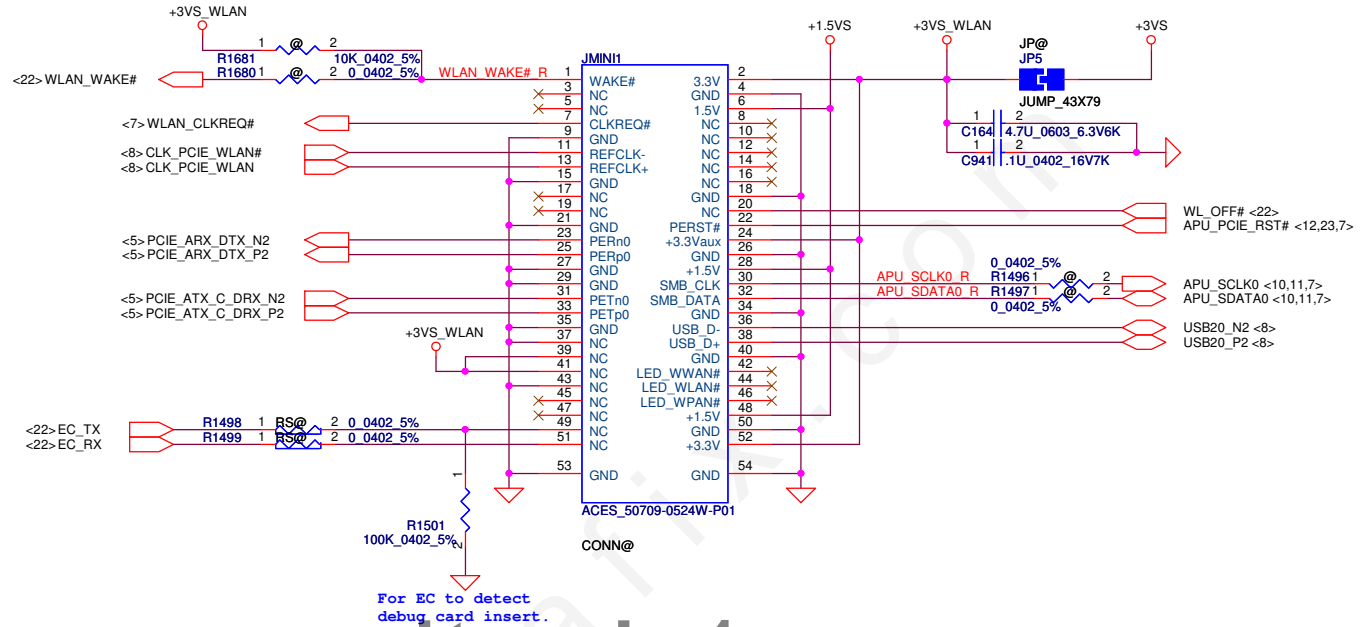
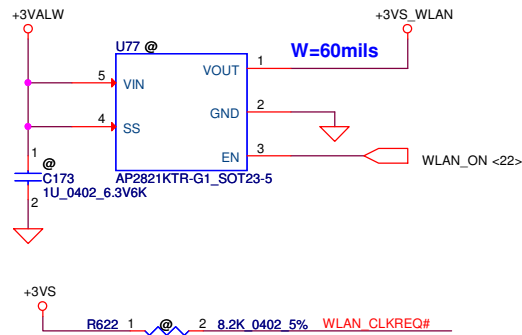
www.aitech1.ru

Card Reader Connector



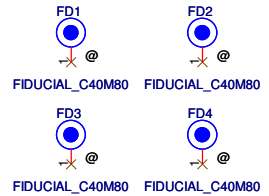
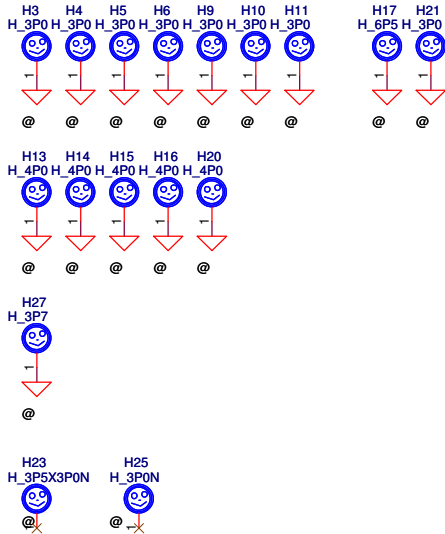
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	LAN RJ45/CR SD Connector	
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Mini-Express Card(WLAN/WiMAX) H=4mm



Use RX for BT off function

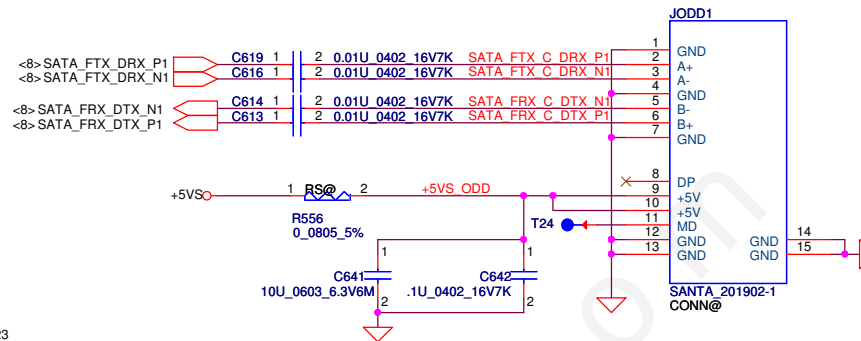
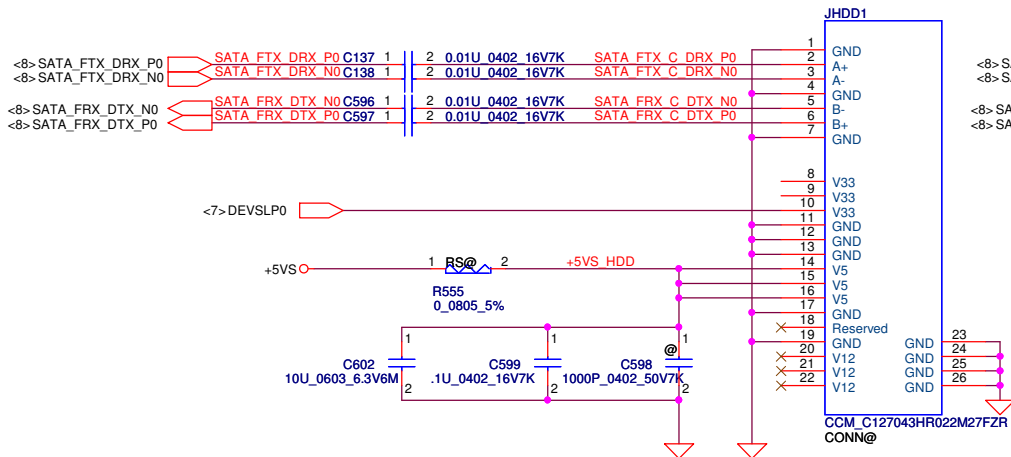
www.aitech1.ru



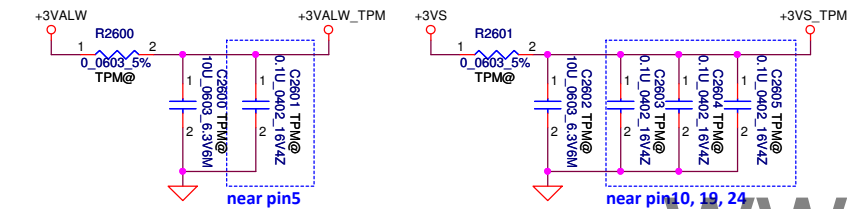
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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	
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SATA HDD Conn.

SATA ODD Conn.



TPM



BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

GPIO3/BADD with Internal PH (default)

AMD CLKRUN# no need PH (DG1.1)

LPCPD# had internal PH

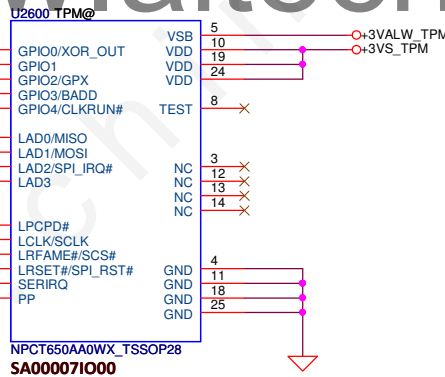
SERIRQ no need PH

CLKRUN# PH request by TPM chip DG 1/22

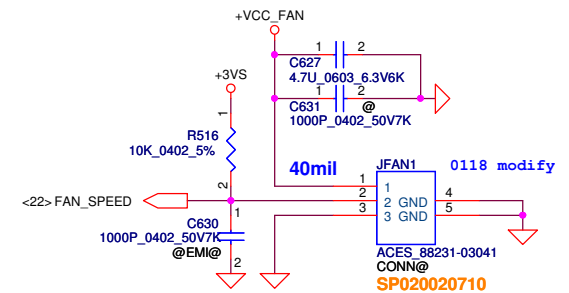
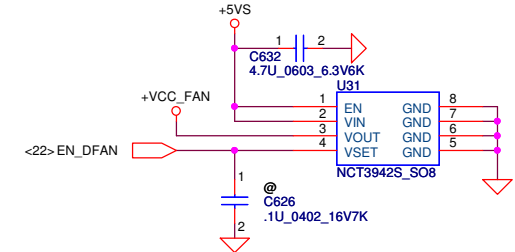
CLKRUN# 10K_0402_5% R2604

close to EC

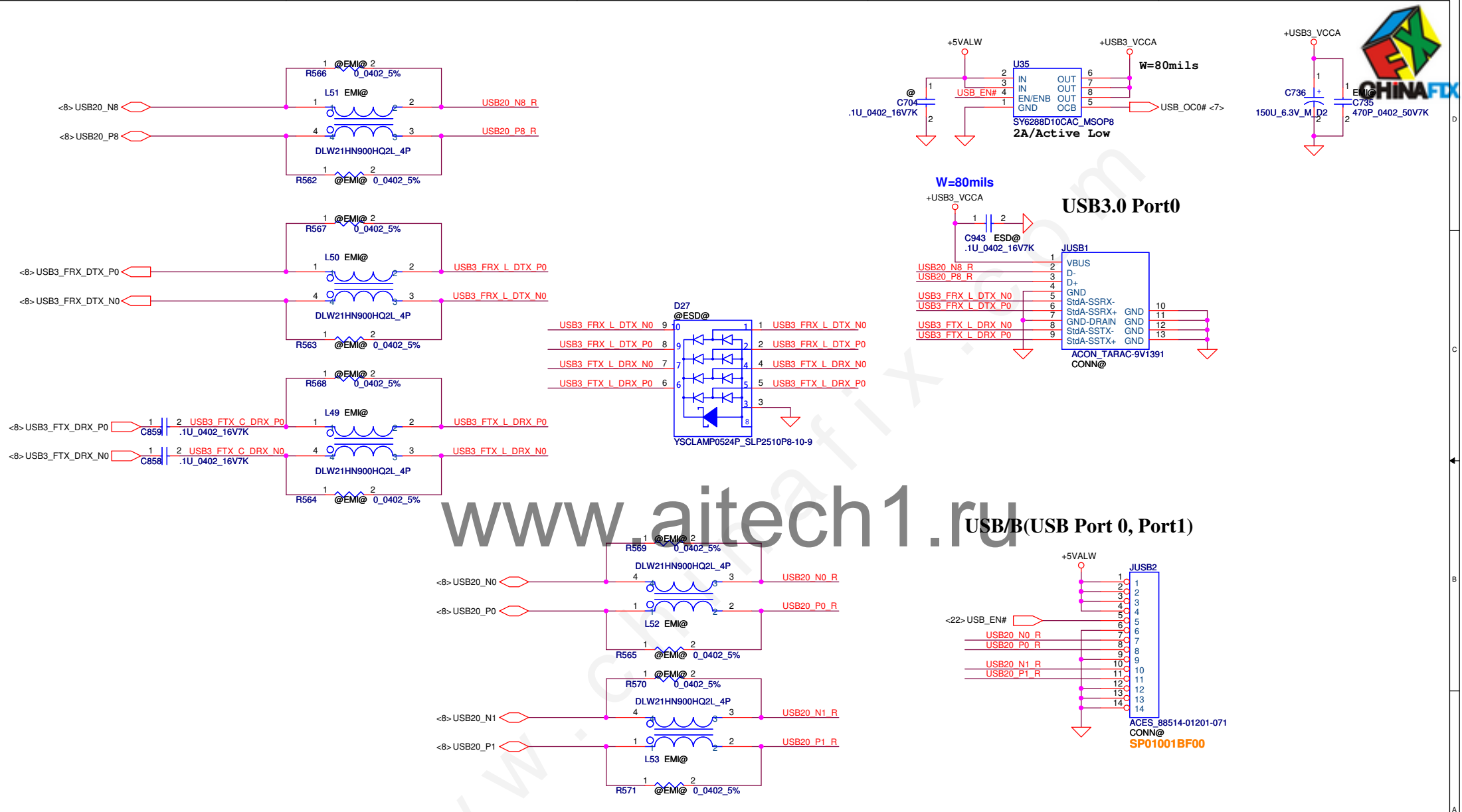
LPC_AD3_R	R1684	1	TPM@	2	0.0402 5%	LPC_AD3
LPC_AD2_R	R1685	1	TPM@	2	0.0402 5%	LPC_AD2
LPC_FRAME#_R	R1686	1	TPM@	2	0.0402 5%	LPC_FRAME#
LPC_AD1_R	R1687	1	TPM@	2	0.0402 5%	LPC_AD1
LPC_AD0_R	R1688	1	TPM@	2	0.0402 5%	LPC_AD0
SERIRQ_R	R1689	1	TPM@	2	0.0402 5%	SERIRQ



FAN Conn



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Date		Sheet		Rev	
Thursday, March 27, 2014		27 of 45		1.0	

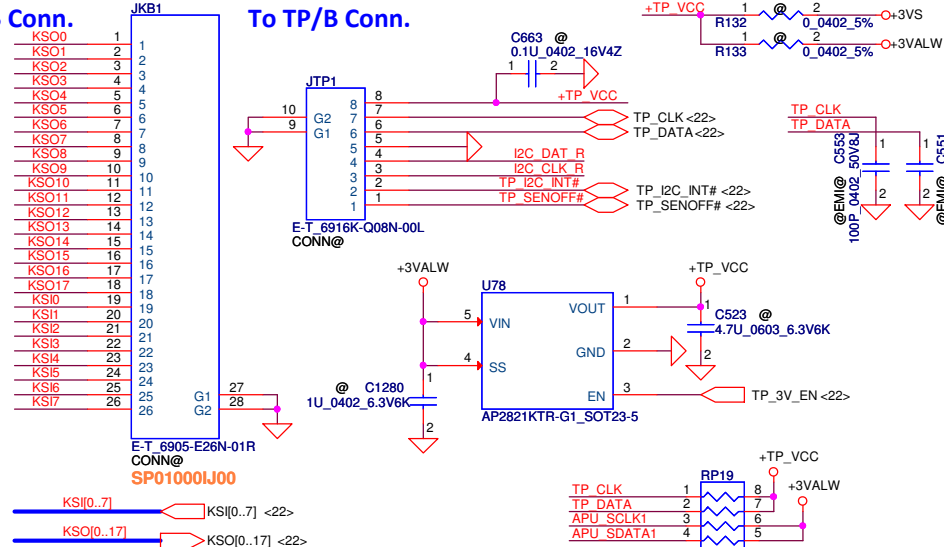


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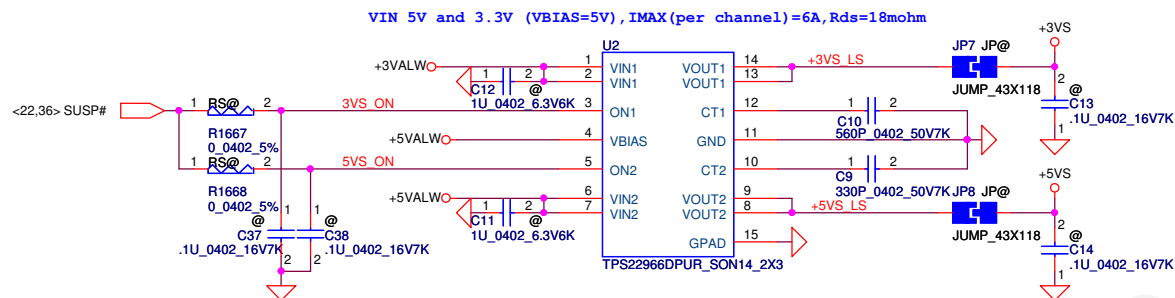
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Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	
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KB Conn.

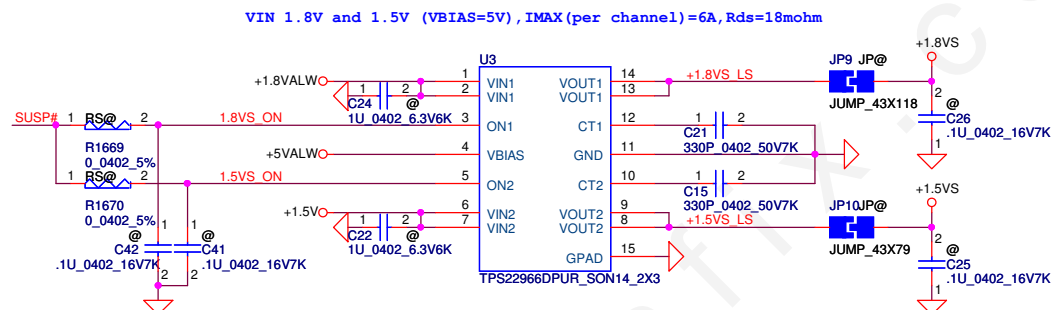
To TP/B Conn.



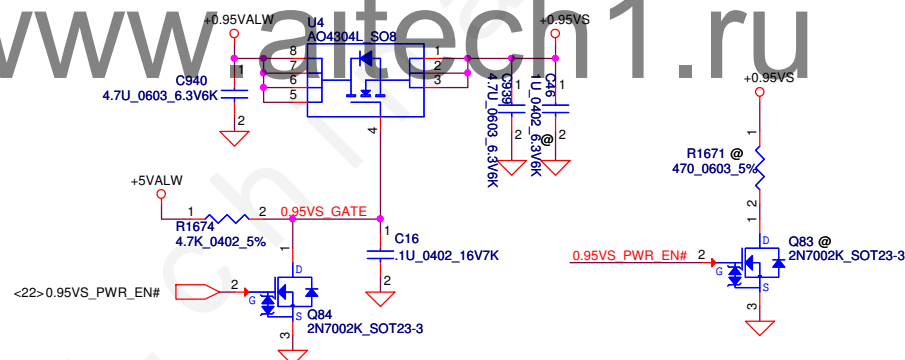
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



+1.8VALW TO +1.8VS
+1.5V TO +1.5VS
Load switch



+0.95VALW to +0.95VS



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0.2

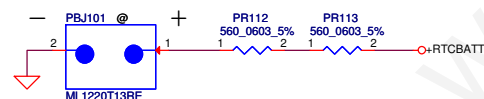
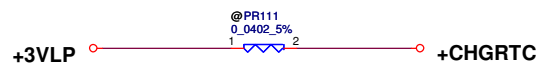
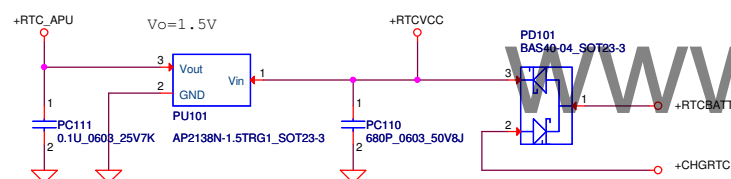
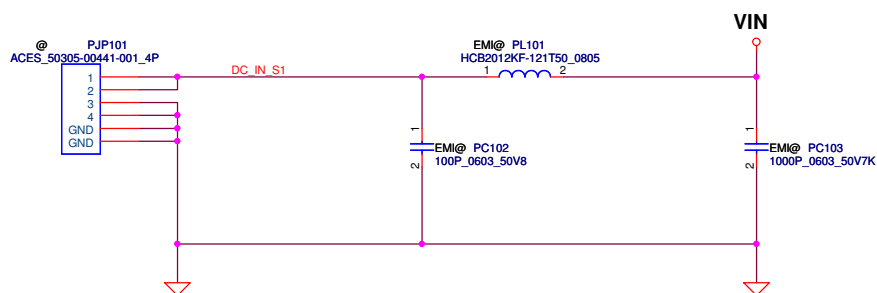
- 1. Add R693 for UMA/DIS select
- 2. Change R756,R765,R769,R779,R781,R782,R783 and R794 to Rshort for EMI request
- 3. Change BID to 1 for DVT
- 4. Change LAN_WAKE# PU to +3V_LAN
- 5. Add L76,L77,C2142 and C2140 for ESD request
- 6. Change R238 and R237 to 59ohm
- 7. Add L52,L53,R565,R569,R570 and R571 for EMI request.
- 8. Add R140,R141,R142,R143,R144 and R145 for reserve USB TP
- 9. Pop Q89, unpop R1690
- 10. Change D10 to SCA00001B00
- 11. Change L11 to SM01000EJ00
- 12. Add U39,R833,C185,R1578 for VGA power sequence issue
- 13. Remove APU_ALERT#_R
- 14. Add C668 and C836 for vendor request

0.3

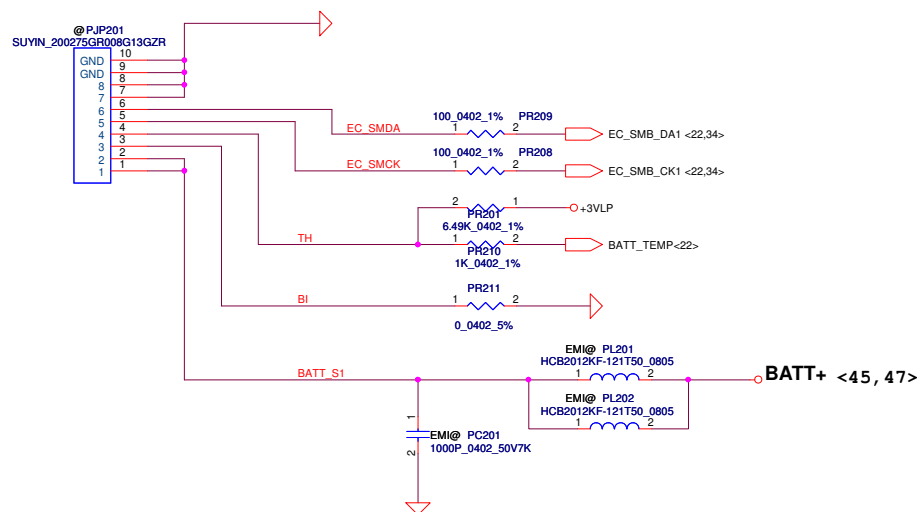
- 1. Change JTP1
- 2. Add U78 for TP +3V power plane
- 3. Change C849, C849 to 10p
- 4. Change C736 to 150u D2 type.
- 5. Change R699, R700 to 330ohm; R698, R701 to 560ohm
- 6. Change U69 +3VALW to +3VS
- 7. Add C366, C367, C368, C369 for EMI request
- 8. Add on board TPM
- 9. Add R619

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				Size	Document Number	Rev
				Z5WAE LA-B231P		1.0
				Date	Thursday, March 27, 2014	
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---Battery_pin define---

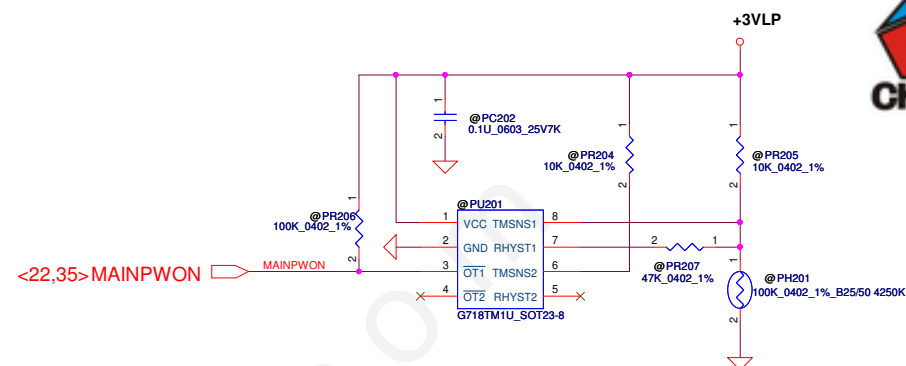
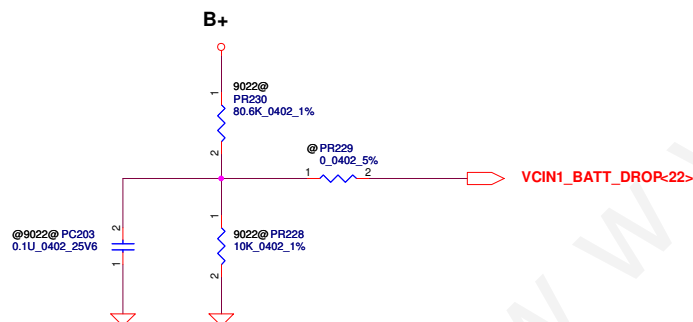
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

---Battery Con_pin define---

PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V



	For KB9012 OTP	For KB9022 OTP
92°C		1.0V
56°C		2.0V
PR216		16.9K ohm

2014/01/02 update

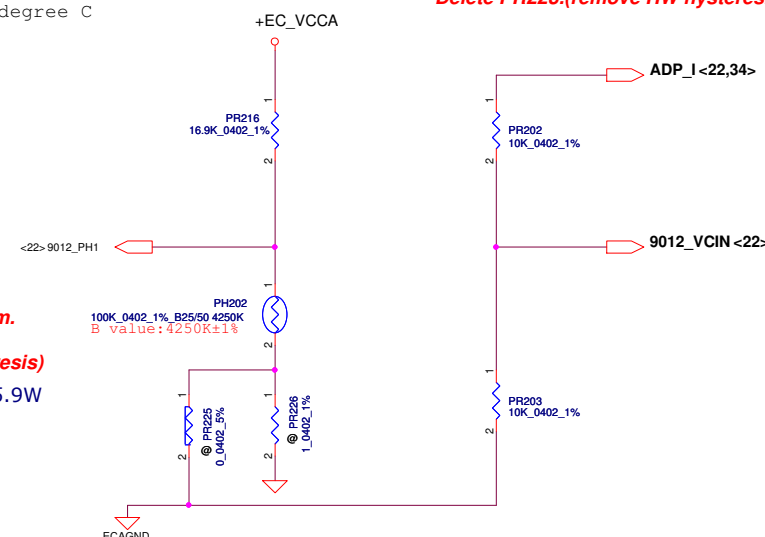
For KB9022 sense 20mΩ	Active	Recovery
65W	70W, 0.73V	55.9W, 0.59V

2013/10/22 Modify
PH201, PH202 change to common part.

2013/12/16 Modify
Delete PR223.(remove HW hysteresis)

PH201 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

2013/10/25 Modify
PR227(9012@) change to 26.1K ohm.
2014/02/07 Modify
Delete @PR227.(remove HW hysteresis)
For 65W adapter==>action 70W , Recovery 55.9W

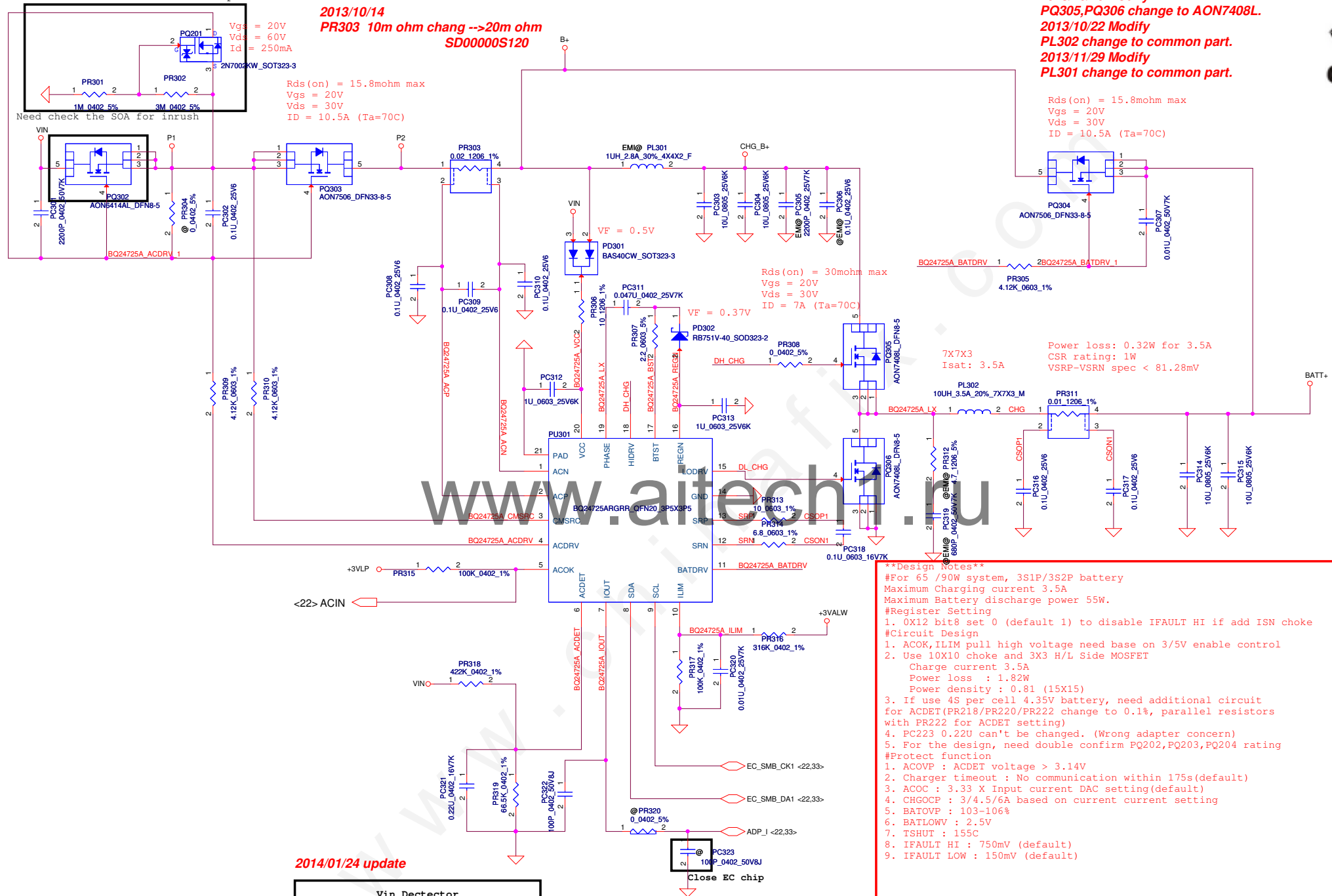


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				Size	Document Number		Rev	
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2013/10/14
PR303 10m ohm chang -->20m ohm
SD00000S120

$R_{ds(on)} = 15.8\text{mohm max}$
 $V_{gs} = 20\text{V}$
 $V_{ds} = 30\text{V}$
 $I_D = 10.5\text{A}$ ($T_a = 70^\circ\text{C}$)

2013/10/16 Modify
PQ305, PQ306 change to AON7408L.
2013/10/22 Modify
PL302 change to common part.
2013/11/29 Modify
PL301 change to common part.



2014/01/24 update

Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

$V_{ILIM} = 20 \times I_{LIM} \times R_{sr}$
 $I_{LIM} = 3.3 \times 100 / (100 + 316) / 20 / 0.01$
 $= 3.966 \text{ A}$

****Design Notes****
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
#Circuit Design
1. ACOK, ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L Side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
4. PC223 0.22u can't be changed. (Wrong adapter concern)
5. For the design, need double confirm PQ202, PQ203, PQ204 rating
#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s (default)
3. ACOC : 3.33 X Input current DAC setting (default)
4. CHGOC : 3/4.5/6A based on current current setting
5. BATOV : 103-106%
6. BATLOW : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 150mV (default)

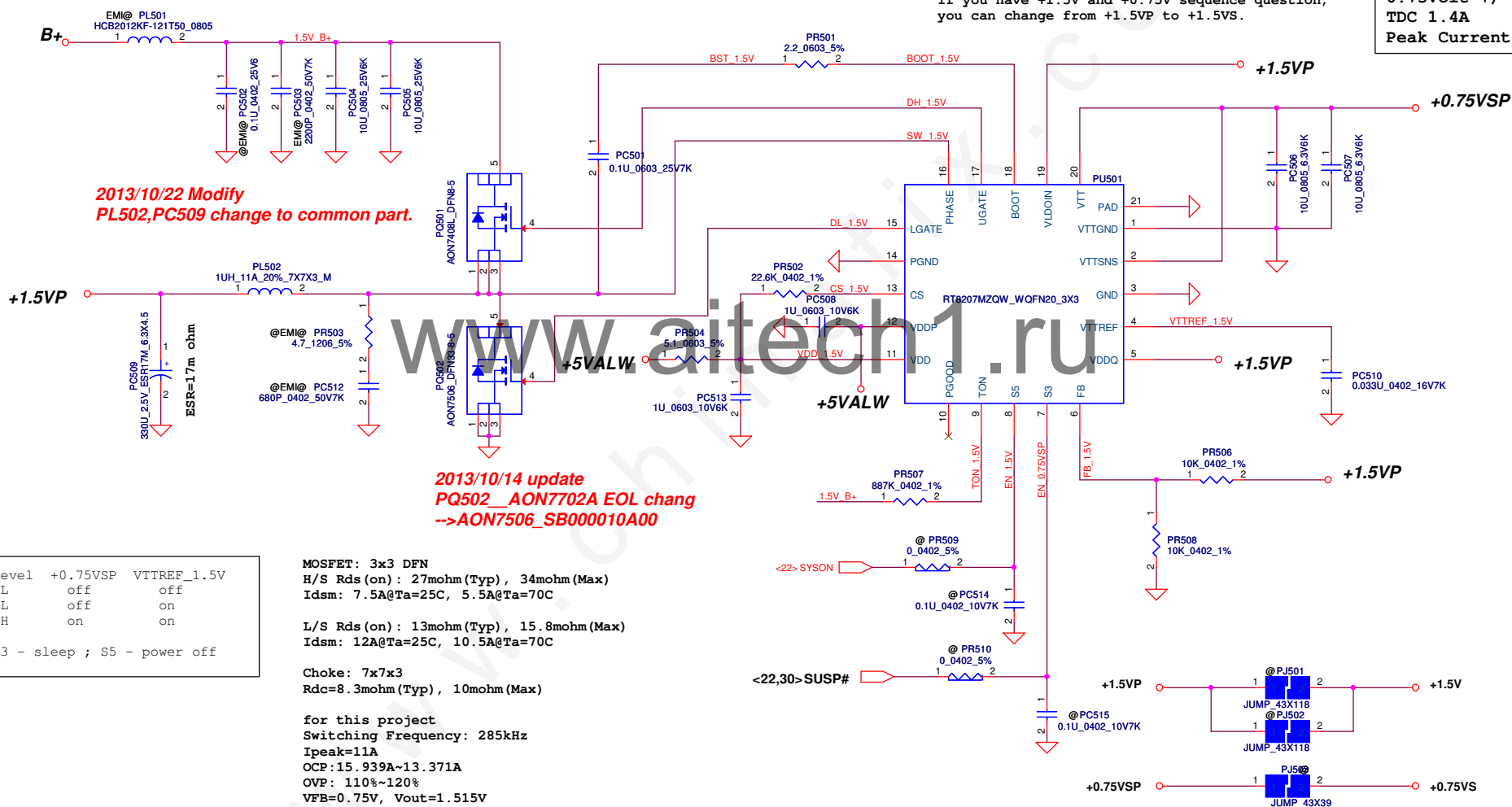
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				Rev	1.0

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 1.4A
Peak Current 2A



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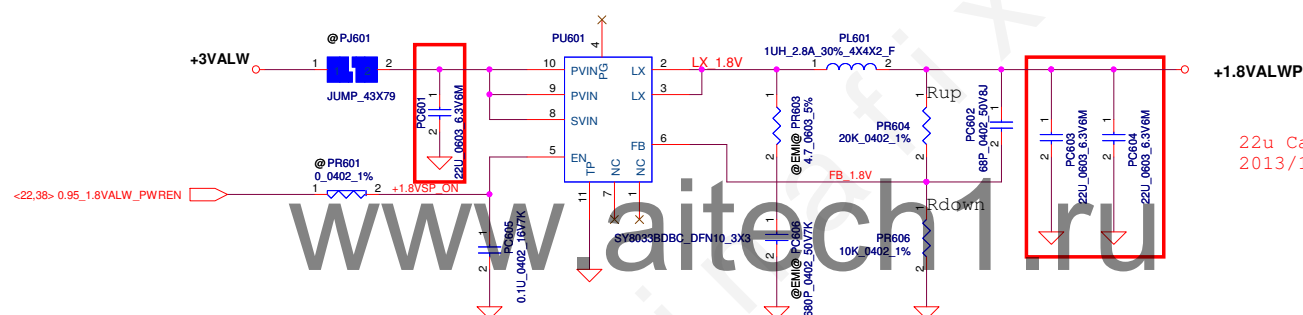
Module model information

SY8033_V1.mdd

22u Capacitor change to 0603 size.
2013/10/16 modify.

2013/10/22 Modify
PL601 change to common part.

FB=0.6V
Note: Iload (max)=3.5A



22u Capacitor change to 0603 size.
2013/10/16 modify.

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

Delete PR605, because same net name have two PD resistor in circuit.
2013/11/29 modify.



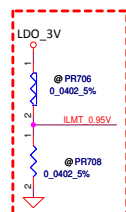
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Module model information

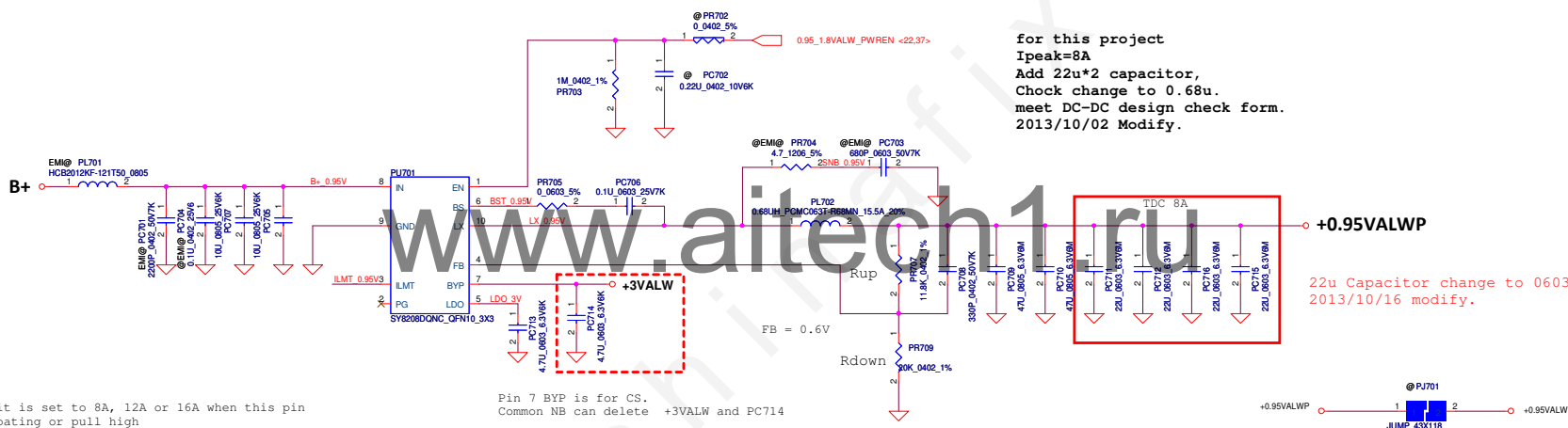
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

for this project
Ipeak=8A
Add 22u*2 capacitor,
Chock change to 0.68u.
meet DC-DC design check form.
2013/10/02 Modify.



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC714

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.954V

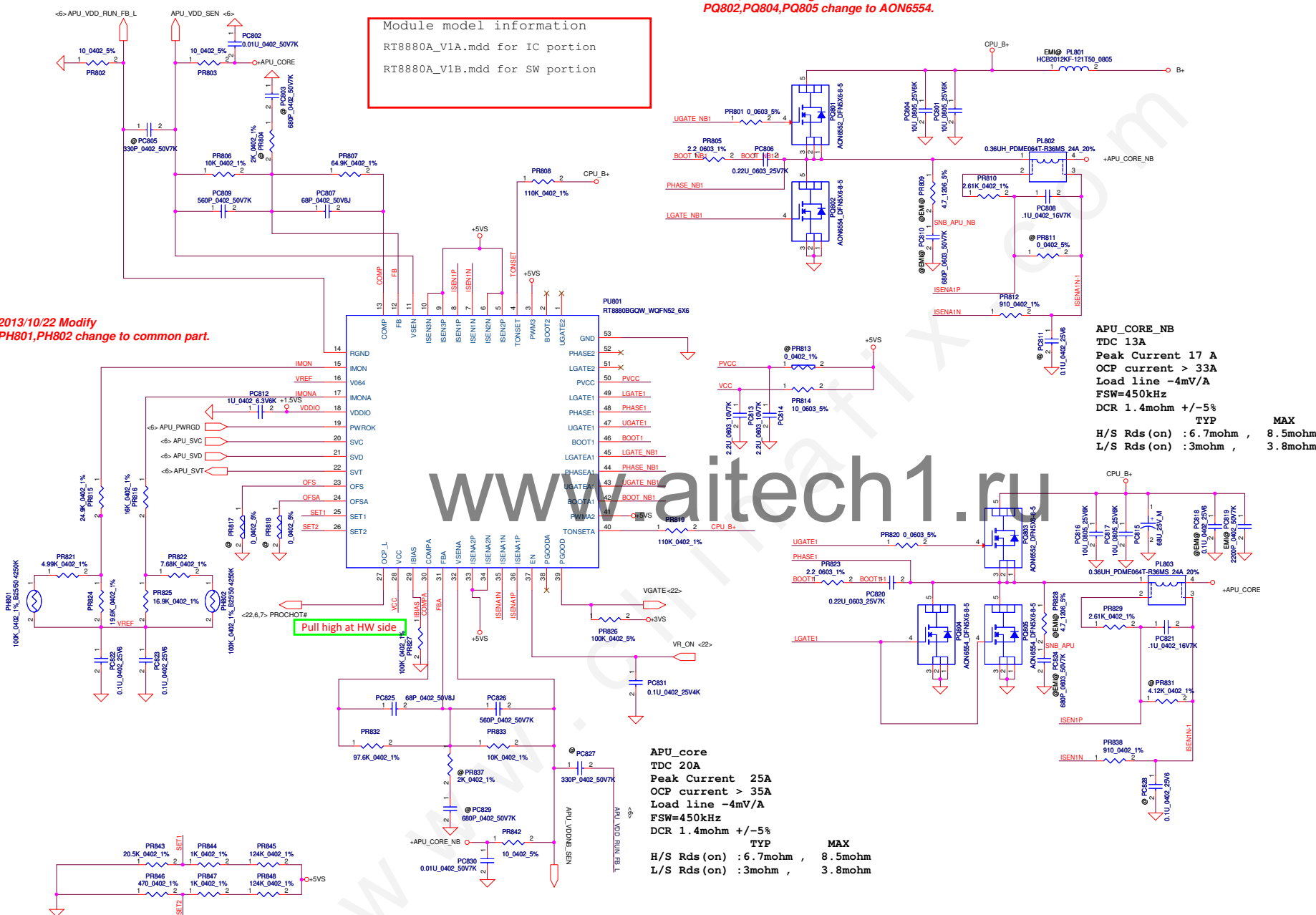
22u Capacitor change to 0603 size.
2013/10/16 modify.

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2013/10/16 Modify
PQ801,PQ803 change to AON6552.
PQ802,PQ804,PQ805 change to AON6554.

Module model information
RT8880A_V1A.mdd for IC portion
RT8880A_V1B.mdd for SW portion

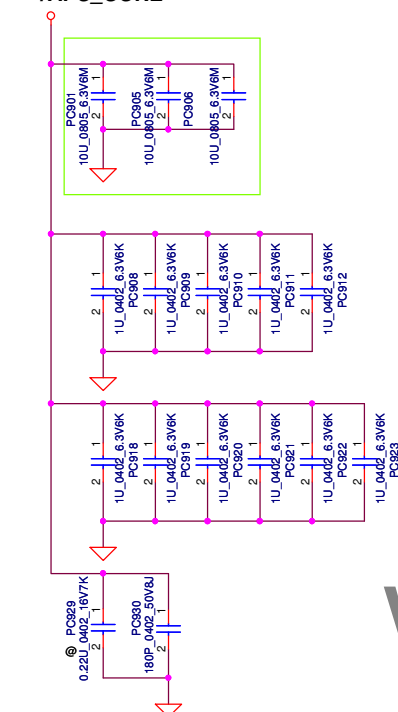
2013/10/22 Modify
PH801,PH802 change to common part.



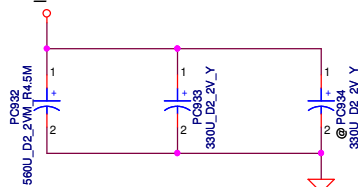
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+APU_CORE (36.4)

+APU_CORE

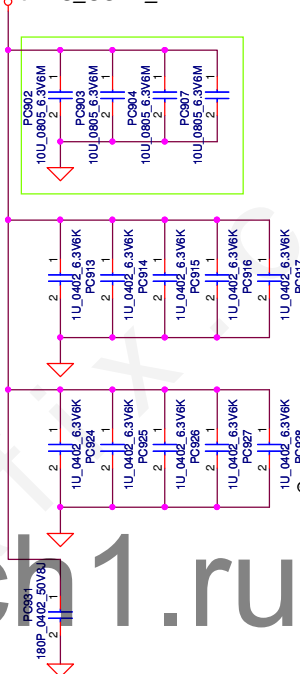


+APU_CORE

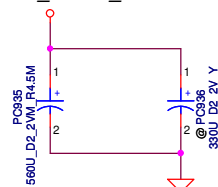


+APU_CORE_NB (36.5)

+APU_CORE_NB



+APU_CORE_NB



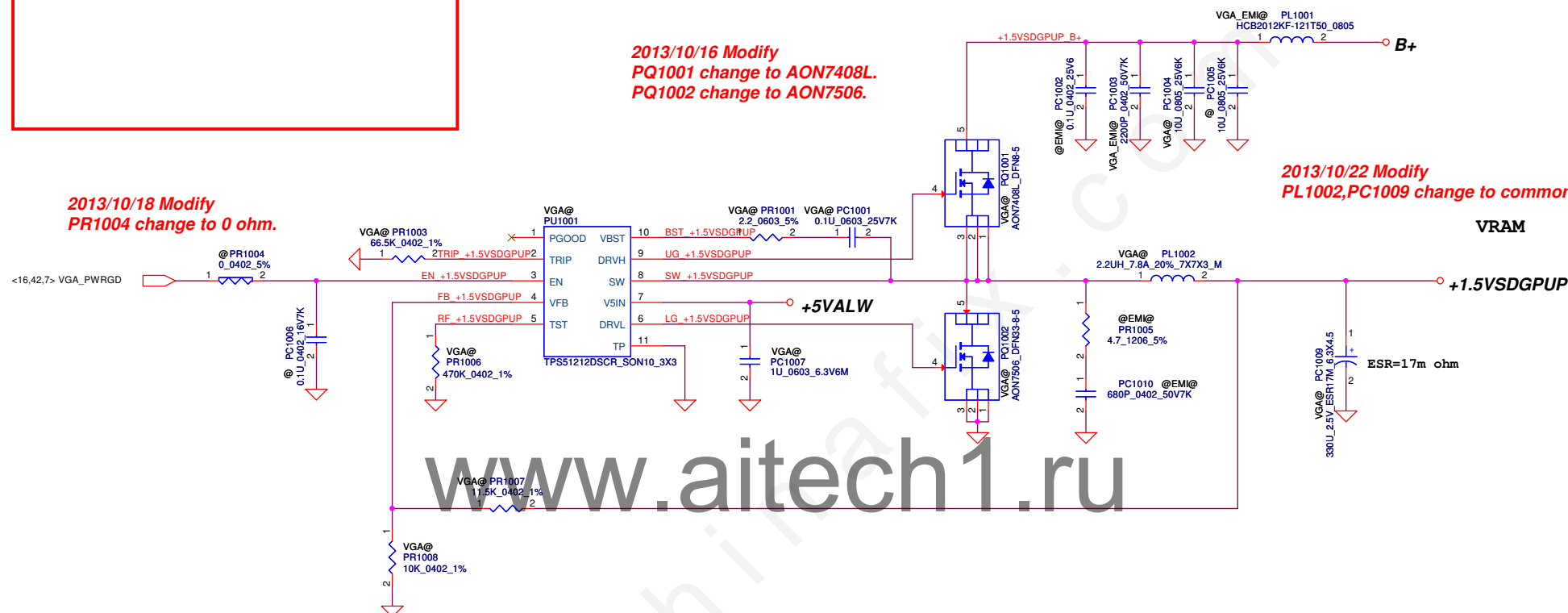
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Module model information
TPS51212_V1.mdd for Single layer
TPS51212_V2.mdd for Dual layer

2013/10/16 Modify
PQ1001 change to AON7408L.
PQ1002 change to AON7506.

2013/10/18 Modify
PR1004 change to 0 ohm.

2013/10/22 Modify
PL1002, PC1009 change to common part.



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

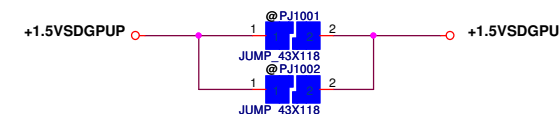
L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Vout	PR1007	PR1008	PR1003
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k
+1.5V	11.5K	10k	105K

+1.5V(for this project)

Switching Frequency: 290kHz
Ipeak=4.7A
OCP: 6.884A~5.751A
OVP: 120%~130%
VFB=0.704V, Vout=1.514V
PR1003=66.5K Ohm



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2013/10/16 Modify
PQ1201,PQ1203 change to AON6552.
PQ1202,PQ1204 change to AON6554.

Remark:
1. PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
=> 2 phase GPU VR config
PWM3 (Pin24) tie to 5V & CLK# (Pin40) tie to GND or floating
=> 2 phase GPU VR config

2. When 2 Phase GPU config
a. DPSLPVR (Pin39)=0 PS# (Pin2)=0
=> 1 phase CCM operation mode
b. DPSLPVR (Pin39)=0 PS# (Pin2)=1
=> 2 phase CCM operation mode
c. DPSLPVR (Pin39)=1 PS# (Pin2)=0 or 1
=> 1 phase DE operation mode

3. Rbias=147K => overshoot reduction function disable
Rbias=47k => overshoot reduction function enable

4. Thermal throttling:
Protect: (6.98K+Rth)*60uA=1.2V
=> Rth=13.02K
=> Tj=110C (+3C) <13> GPU_DPSLPVR
Recovery: (6.98K+Rth)*56uA=1.24V
=> Rth=15.16K
=> Tj=105C (+3C)

5. Switching frequency set :
Rfset(kohm)=period(us)*0.29*2.65
=5.9Kohm
fsw=1/period(us)=400KHZ

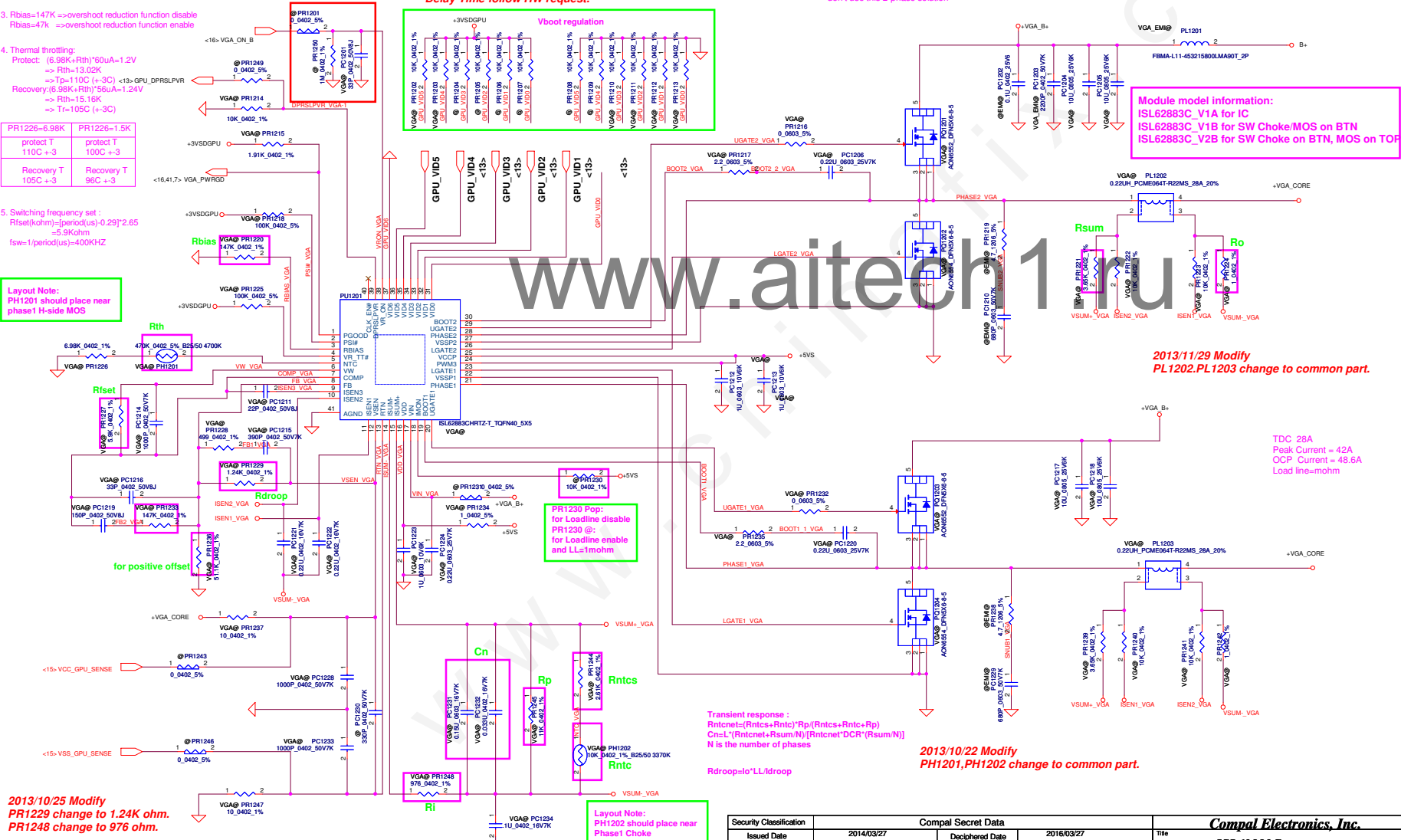
Layout Note:
PH1201 should place near
phase1 H-side MOS

2013/10/25 Modify
PR1229 change to 1.24K ohm.
PR1228 change to 976 ohm.

"Jet Type"

2013/10/18 Modify
EN Signal change to VGA_ON.
Delay Time follow HW request.

2013/11/29 Modify
Delay Time follow HW request.
Add PD Resistor(PR1250)
2013/12/16 Modify
Delay Time follow HW request.



	AMD MARS series				AMD SUN series			Description
	LP: DDR3 PioXT/XTX: GDDR5				UL: DDR3 PioXT/XTX: GDDR5			
GPU	MARS XTX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	NA
VDDC	0.775-1.175V	0.775-1.125V	0.775-1.050V	0.775-1.000V	0.775-1.125V	0.800-1.075V	0.800-1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCP	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	-----	-----	-----	1mohm	NA
Ri	1.13K Ohm	887 Ohm	750 Ohm	-----	-----	-----	887 Ohm	for OCP and LoadLine Setting
Rdroop	1.43K Ohm	1.13K Ohm	953 Ohm	-----	-----	-----	1.13K Ohm	for LoadLine Setting
PR1229	187K Ohm	147K Ohm	124K Ohm	-----	-----	-----	147K Ohm	for Compensation
PR1233	51.1K Ohm	51.1K Ohm	51.1K Ohm	-----	-----	-----	51.1K Ohm	for Positive offset
PR1236	51.1K Ohm	51.1K Ohm	51.1K Ohm	-----	-----	-----	51.1K Ohm	for Positive offset

Remark: MARS LP/ SUN UL/ SUN PRO
don't use this 2-phase solution

MOS TYP MAX
H/S Rds(on) : 6.7mohm , 8.5mohm
L/S Rds(on) : 3mohm , 3.8mohm
Choke: 0.22uH (Size:7774)
Rdc=0.98mohm +5%
Heat Rating Current=28A
Saturation Current=28A

Module model information:
ISL62883C_V1A for IC
ISL62883C_V1B for SW Choke/MOS on BTN
ISL62883C_V2B for SW Choke on BTN, MOS on TOP

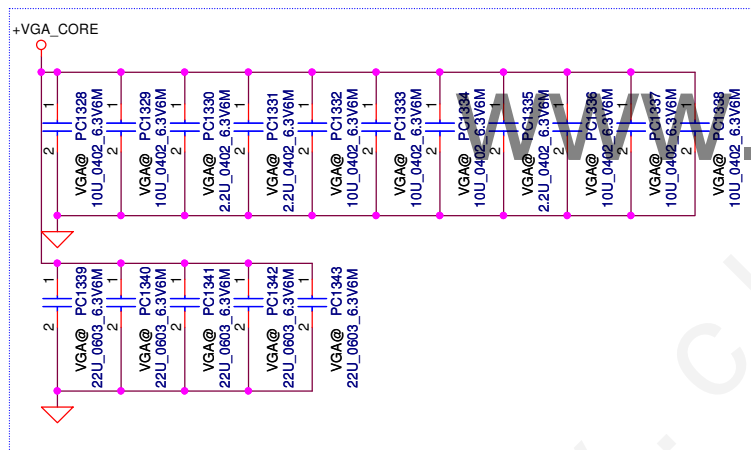
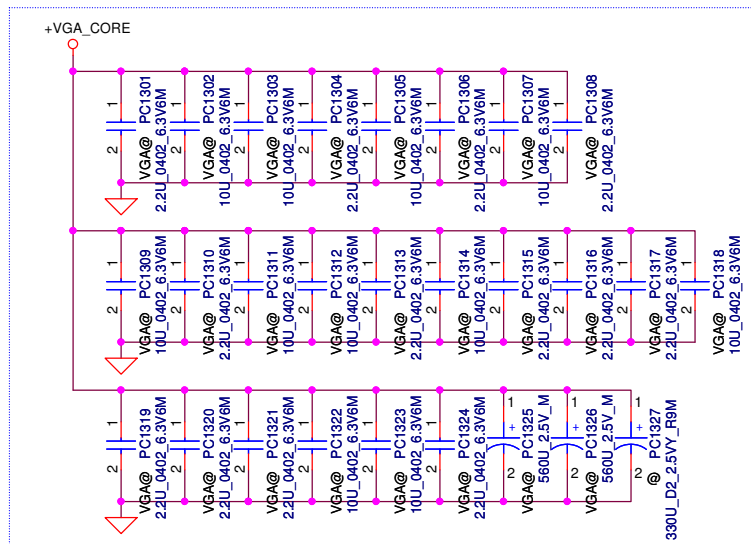
2013/11/29 Modify
PL1202,PL1203 change to common part.

TDC 28A
Peak Current = 42A
OCP Current = 48.6A
Load line=mohm

2013/10/22 Modify
PH1201,PH1202 change to common part.

Transient response :
 $R_{ntc} = (R_{ntc1} + R_{ntc2}) * R_p / (R_{ntc1} + R_{ntc2} + R_p)$
 $C_{nL} = L * (R_{ntc1} + R_{ntc2} + R_p) / (R_{ntc1} * R_{ntc2} * R_p)$
N is the number of phases
Rdroop=Lo*Ldroop

Layout Note:
PH1202 should place near
Phase1 Choke



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Version change list (P.I.R. List)

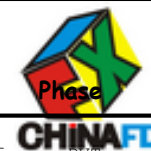
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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	
1	Design Change.	Design Change of Diode Application.	0.2	32	Change PD101 to SCSS4004010(S SCH DIO BAS40-04 SOT23).	2013/11/29	DVT
2	Design Change.	Design Change of IC Application.	0.2	35	Add non-pop component PC427,PC428.	2013/11/29	DVT
3	Design Change.	reduce part count.	0.2	37	Delete PR605 PD resister.	2013/11/29	DVT
4	Design Change.	reduce part count.	0.2	39	Delete @PR834.@PR835.@PR836.@PR839.@PR840.@PR841.	2013/11/29	DVT
5	Design Change.	Design Change of VGA Type Application.	0.2	42	PR1205 change to non-pop. PR1211 change to pop.	2013/11/29	DVT
6	Design Change.	Design Change of common part.	0.2	34	Change PL301 to SH00000YG00 (S COIL 1UH +-30% 2.8A 4X4X2 FERRITE).	2013/11/29	DVT
7	Design Change.	Design Change of common part.	0.2	42	Change PL1202.PL1203 to SH000011H00 (S COIL .22UH +-20% 24A 7X7X4 MOLDING).	2013/11/29	DVT
8	Design Change.	Design Change of Delay Time.	0.2	42	Change PR1201 to SD028000080(S RES 1/16W 0 +-5% 0402). Change PC1201 to non-pop.	2013/11/29	DVT
9	Design Change.	Design Change of EC Type Application.	0.2	35	Add PD101 SCS00000200(S SCH DIO RB751V-40 SOD-323).	2013/11/29	DVT
10	Design Change.	Design Change of Circuit Application.	0.2	42	Add PR1250 SD034100480(S RES 1/16W 1M +-1% 0402).	2013/11/29	DVT
11	Design Change.	Design Change of Delay Time.	0.2	42	Change PR1201 to SD028000080(S RES 1/16W 0 +-5% 0402). Change PC1201 to SE071330J80(S CER CAP 33P 50V J NPO 0402)	2013/12/16	DVT
12	Design Change.	Design Change of Circuit Application.	0.2	33	Delete PR223.(remove HW hysteresis)	2013/12/16	DVT
13	Design Change.	Design Change of Circuit Application.	0.2	42	Change PR1250 to non-pop.	2013/12/16	DVT
14	Design Change.	Design Change of Circuit Application.	0.2	34	Change PQ303,PQ304 to SB000010A00(S TR AON7506 1N DFN).	2013/12/19	DVT
15	Design Change.	Design Change of Circuit Application.	0.2	33	Add PL202 SM01000C000 (S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2013/12/19	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
16	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR211 to SD028000080(S RES 1/16W 0 +-5% 0402).	2013/12/25	DVT
17	Design Change.	Design Change of Circuit Application.	0.2	35	Change PC426 to pop.	2013/12/25	DVT
18	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR216 to SD034162280(S RES 1/16W 16.2K +1% 0402).	2013/12/25	DVT
19	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR216 to SD034169280(S RES 1/16W 16.9K +-1% 0402).	2014/01/02	DVT
20	Design Change.	Design Change of Circuit Application.	0.2	33	Change PR202 to SD034100280(S RES 1/16W 10K +-1% 0402).	2014/01/02	DVT
21	Design Change.	Design Change of Circuit Application.	0.3	37.38. 39.41.	Change PR813,PR601,PR706,PR702,PR1004 to SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT
22	Design Change.	Design Change of Circuit Application.	0.3	35	Remove PD401. Add @PR410 SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT

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